6th IEEE International Conference on
VLSI Systems, Architecture, Technology and Applications
(VLSI SATA), June 12-13, 2026

Venue: ***Amrita Vishwa Vidyapeetham, Amrita School of Engineering, Bengaluru***

https://www.amrita.edu/events/vlsi-sata-2026/

The 6th IEEE VLSI SATA (Systems Architecture, Technology and Applications) conference would promote knowledge building, engineering education, research and development activities, and networking to establish and identify research groups and collaboration opportunities. The 6th edition of VLSI SATA is scheduled during June 12-13, 2026. The theme of the conference is "VLSI with AI/ML Applications". The conference is jointly organized and hosted by Amrita School of Engineering (ASE), Bengaluru in collaboration with IEEE Circuit and Systems Society (CASS), Bengaluru.

IMPORTANT DATES

Paper Submission Deadline:
28th February, 2026
Notification of Acceptance:
15th April, 2026
Camera Ready:
30th April, 2026

CALL FOR WORKSHOP, TUTORIAL, INVITED PAPERS
SUBMISSION DEADLINE: 28/02/2026

CALL FOR WORKSHOPS

Workshops proposals are invited from industrial experts to be held alongside the main conference. The length of the workshops can be half day or full day. The following information is required from workshop organizers. Organizers details like Name, Designation, Affiliation, Title of the workshop, Abstract, Brief profile of organizer(s), Photograph, Length of the workshop, Targeted audience, Plan for attracting audience, etc. Please submit the workshop proposal in pdf format via mail

Please contact workshop chair for any queries:

Dr. Phani Raj Harivanam: r_phani@blr.amrita.edu
Dr. Shivalila A Hangaragi: h_shivalila@blr.amrita.edu
Dr. Patthi Aruna:p_aruna@blr.amrita.edu

CALL FOR TUTORIALS

Tutorials are invited from experts to be conducted in association with the main conference. The length of the tutorial can be half day or full day. In-depth tutorial on emerging topics may attract more participants. The following information is required from tutorial speaker(s). Details like Name, Designation, Affiliation, Title of the tutorial, Abstract, Photograph, Length of the tutorial, Targeted audience, etc. Please submit the tutorial proposal in pdf format via mail

Please contact tutorial chairs for any queries:

Dr. R.V. Sanjika Devi: r_sanjika@blr.amrita.edu
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CALL FOR INVITED PAPERS

Invited papers are requested from experienced authors who are experts in the domain.The paper format and template remain the same as regular IEEE conference template. The invited paper will also be submit- ted to IEEE Xplore. Please submit the invited papers in pdf format via CMT submission page-

https://cmt3.research.microsoft.com/VLSISATA2026/Submission/Index

Please contact Program Chairs for any query:

Dr. Manoj Kumar Panda: kp_manoj@blr.amrita.edu
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For more details, please visit at
https://www.amrita.edu/events/vlsi-sata-2026/
or
scan us

CONTACT US

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VLSI SATA 2026 will feature the presentation and discussion of new findings in the theory, methodology, design, and applications of VLSI. It serves as a global forum for researchers, academicians, and practitioners to share their ongoing theoretical research endeavours, innovative system and design solutions and practical VLSI applications. The conference program includes traditional paper presentations, engaging workshops, and keynote addresses by distinguished experts and authorities.

CALL FOR PAPERS

Prospective authors are invited to submit their full and original research papers in IEEE format, with the requirement that these papers should not have been submitted, published, or under consideration in any other conferences or journals.

SYSTEMS

- Reliable and/or Safe Embedded Electronics
- Systems for Testing
- Digital System Design and Validation
- Digital System and Circuits
- Memory Subsystems
- Memory Computing Systems
- HW/SW Co-design
- IoT Systems
- Cyber Physical Systems
- Embedded Operating Systems
- Analog and Mixed Signal Systems
- RF Circuits and Systems
- Low Power Systems
- Power Management Systems
- Data Converters
- High Speed Interfaces
- Reliable Systems
- Wireless Circuits and Systems
- CAD Tools and Methodologies for Design and Optimization

ARCHITECTURE

- Inter-chip Interconnect
- On-chip Interconnect
- Multicore and Manycore
- Data Centric Architecture
- System on Chip
- Embedded Processor Architecture in Vehicles
- High-performance Computing
- Embedded FPGA Reconfigurable Computing
- Built In Self Test (BIST)
- Design for Test Fault Tolerance
- Quantum Computing
- Network Security
- Side-channel and Fault Analysis
- Trusted Computing
- Hardware Trojan
- Functional Safety and Privacy
- Optical Interconnect Architecture
- Reliable Communication Architecture
- NoC for FPGA, ASIC, CMP and MPSoC
- Approximate Computing

TECHNOLOGY

- 3D ICs
- MEMS, GaN, and SiC devices
- Layout Technology
- Physical Design
- Interconnect Technologies
- 3D Packaging and Wafer-level Packaging
- New Age Nanoelectronic Devices
- Electronic Design Automation
- Advanced CMOS Technology
- Advanced Packaging and Heterogeneous Integration Technology
- Process Technology

APPLICATIONS

- IoT and Big Data Analytics
- AI-oriented Applications
- Video and Image Processing
- Applications Hardware Security and Trust
- ML-oriented Applications
- Wireless/Wired Communication Networks
- Automotive and Vehicular Networks
- RF Energy Harvesting
- Power Electronics Applications
- Biomedical and Healthcare Applications
- Sensors and Instrumentation Applications
- Signal Integrity Applications

SUBMISSION

Paper submission is through CMT paper management systems. If you already have CMT login; you can make use of that otherwise, you may need to create a login for Microsoft CMT.

https://cmt3.research.microsoft.com/VLSISATA2026/Submission/Index

Manuscript Preparation

Authors can submit their manuscript properly formatted as pdf file. Please find the template and author guidelines here.
https://www.ieee.org/conferences/publishing/templates.html
Use US Letter size in the case of MS Doc.

Page Length

Maximum manuscript length should be 6 pages. (Extra 1-2 page would cost significantly high amount). The paper must include an abstract of about 150 words and a maximum of five keywords. Review/Survey paper is normally discouraged to be submitted in the conference.

PREVIOUS PUBLICATIONS

2015 :https://ieeexplore.ieee.org/xpl/conhome/7044910/proceeding
2016: https://ieeexplore.ieee.org/xpl/conhome/7586733/proceeding
2022: https://ieeexplore.ieee.org/xpl/conhome/10046417/proceeding
2024: https://ieeexplore.ieee.org/xpl/conhome/10560064/proceeding
2025: https://ieeexplore.ieee.org/xpl/conhome/11069443/proceeding

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