Department of Electronics and Communication Engineering

Amrita School of Engineering

Amrita Vishwa Vidyapeetham

M.Tech Programme in VLSI Design

About Amrita

Amrita Vishwa Vidyapeetham is a multi-disciplinary, research-intensive, private university, educating a vibrant student population of over **24,000** by **1700+** strong faculty. Accredited with the highest possible 'A++' grade by NAAC, Amrita offers more than 250 UG, PG, and Ph.D. programs in Engineering, Management, and Medical Sciences including Ayurveda, Life Sciences, Physical Sciences, Agriculture Sciences, Arts & Humanities, and Social & Behavioral Sciences.
With seven campuses at Amaravati, Amritapuri, Bengaluru, Chennai, Coimbatore, Kochi, and Mysuru and a new upcoming campus at NCR Delhi (Faridabad) and spread over 1200+ acres with 10 million square feet of built-up space, Amrita is one of India's top-ranked private universities. Amrita has emerged as the seventh ranked university in the National Institutional Ranking Framework (NIRF) Rankings 2024.

About the Department

The Department of Electronics and Communication Engineering, one of the oldest in the University, offers technology-oriented courses to create manpower in crucial areas, in line industrial expectations. The vision of the department is to mould tomorrow's technocrats, imbibing the essence of human values, for innovation and creativity in science and technology, towards building a peaceful self-sustaining nation. The department also aims at setting standards in teaching and learning for providing a bright career path for the students and to establish itself as a center of excellence in research.

About M.Tech Programme in VLSI Design

Very Large Scale Integrated (VLSI) Circuit Design is setting the benchmark for the growth of technology. M. Tech in VLSI Design addresses the state-of-the-art design technology using computer-aided design (CAD) tools and associated hardware. The course demands learning the principles of VLSI design and fabrication, understanding the complete design flow and developing expertise to design CMOS chips for industrial requirements. The programme lays the foundation for career opportunities in leading VLSI design industries, research labs, and reputed national and international organizations.

Salient Features:

The salient features of the programme include:

- Experienced domain-specific faculty
- Excellent infrastructure with fully equipped laboratories
- Seminars / Expert lectures / Webinars
- Industry relevant Projects
- Student publications
- Integrated M.Tech + Ph.D Programmes
- Opportunities at partner Universities abroad
- Placements and Internships

Students are exposed to various design software tools in this programme. Also, they learn to design, simulate, implement and test complex digital systems using FPGAs (Field Programmable Gate Arrays). Students are trained in several topics that cut across different domains, starting from the lowermost level of physical devices to the top level of application development. Expertise across different domains of VLSI design flow such as VLSI architecture & design, testing and verification, and device technology is a major highlight of the programme. Current focus areas include hardware security, VLSI architectures for signal processing, CAD for VLSI, high frequency CMOS design and modelling, low power VLSI and timing analysis. Ample scope exists for pursuing interdisciplinary research through collaboration and exchange programmes with various national and international institutions.

Vision:

The M.Tech VLSI Design program envisions producing leaders equipped with cutting-edge skills and ethical values, fostering innovation, industry collaboration, and global perspectives for sustainable advancement in integrated circuit design and technology.

Mission:

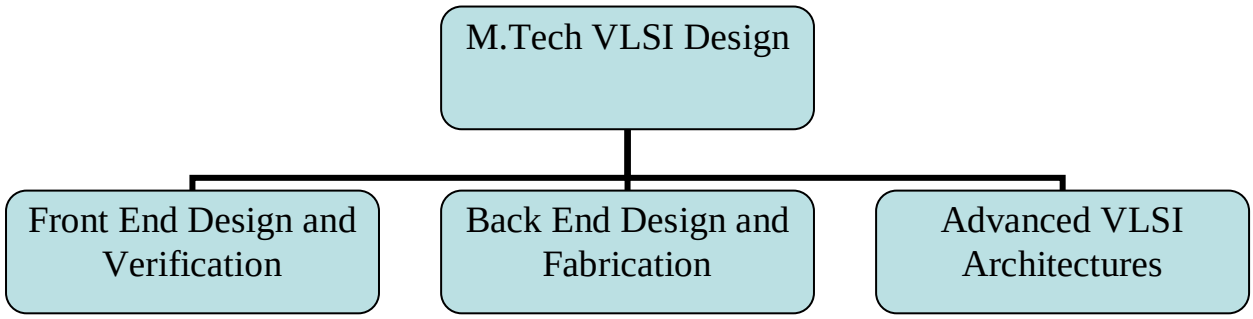
- To equip students with advanced technical knowledge and skills in VLSI design.
- To promote innovation by encouraging students to come up with novel ideas and solutions.
- To enable collaboration with industry partners through Internships, industrial lectures and sharing of practical expertise.
- To cultivate a global perspective, for our students through our international partner universities by Internships, Dual degree programs and research opportunities.

Programme Educational Objectives (PEOs)

PEO1	To create manpower who have attained mastery in applying VLSI concepts to engineering problems in electronics, communication and computing so as to meet the needs of the industry, academia and research.
PEO2	To develop state-of-the-art in VLSI Design to deal with design, development, analysis, testing and evaluation of the critical aspects of integrated circuits and their core concepts.
PEO3	To exhibit professional competence and leadership qualities with a harmonious blend of ethics, leading to the development of an integrated personality.

Programme Outcomes (POs)

PO1	An ability to independently carry out research /investigation and development work to solve practical problems.
PO2	An ability to write and present a substantial technical report/document.
PO3	An ability to demonstrate a degree of mastery in VLSI Design.
PSO1	Ability to demonstrate deep understanding of the principles, theories, and methodologies in VLSI Design, leading to specializations in Front-end design, Verification, Back-end design, Fabrication, and Advanced Architectures.
PSO2	An ability to use modern tools to solve complex problems in design, development, and implementation of VLSI systems.
PSO3	An ability to engage in independent and life-long learning in the context of technological change and industrial demands in VLSI Design.



Curriculum

Semester – I

Type	Code	Course Name	Teaching Schemes			Credits
			L	T	P	
FC	25VL601	Semiconductor Device Modelling	3	0	0	3
SC	25VL602	CMOS Digital Integrated Circuits	3	0	0	3
SC	25VL603	Digital Circuits and Systems	3	0	0	3
SC	25VL604	Analog VLSI Circuits	3	0	0	3
SC	25VL605	Computer Aided Design for VLSI Circuits	3	0	0	3
SC	25VL681	Analog VLSI and device modelling Lab	0	0	3	1

SC	25VL682	RTL design and FPGA Synthesis Lab	0	0	3	1
HU	22ADM501	Glimpses of Indian Culture	0	0	3	P/F
HU	23HU601	Career Competency- I	0	0	3	P/F
HU	25AVP501	Mastery Over Mind (MAOM)	1	0	2	2
		Total	16	0	11	19

Semester – II

Type	Code	Course Name	Teaching Schemes			Credits
			L	T	P	
SC	25VL611	Functional Verification with Hardware Description Languages	3	0	0	3
SC	25VL612	Digital VLSI Testing & Testability	3	0	2	4
E		Elective I	3	0	0	3
E		Elective II	3	0	0	3
E		Elective III	3	0	0	3
SC	25VL683	ASIC front end and back-end Design Lab	0	0	3	1
SC	25VL684	Functional Verification Lab	0	0	3	1
SC	25RM604	Research Methodology	2	0	0	2
HU	23HU611	Career Competency – II	0	0	3	1
SC	25VL698	Industry Internship*	0	0	2	1
		Total	17	0	13	22

***** *The internship will be during the break between the second and third semesters. This will be evaluated based on a viva-voce and a written report.*

Semester – III

Type	Code	Course Name	Teaching Schemes			Credits
			L	T	P	
P	25VL798	Dissertation- Phase I	0	0	30	10
		Total	0	0	30	10

Semester – IV

Type	Code	Course Name	Teaching Schemes			Credits
			L	T	P	
P	25VL799	Dissertation – Phase II	0	0	45	15
		Total	0	0	45	15

Total Credits: 66

Evaluation Pattern:

All courses will follow the evaluation pattern mandated by the university.

Elective courses:

Front End Design and Verification

Code	Course Name	Teaching Schemes			Credits
		L	T	P	
25VL731	Semiconductor Memory Design	3	0	0	3
25VL732	Mixed Signal VLSI Design	3	0	0	3
25VL733	CMOS RF IC Design	3	0	0	3
25VL734	FPGA based System Design	3	0	0	3
25VL735	Electronic System Level Design	3	0	0	3
25VL736	Low Power VLSI Circuit Design	3	0	0	3
25VL737	System-on-Chip & FPGA Testing	3	0	0	3
25VL738	Hardware Security and Design for Trust	3	0	0	3

Back End Design and Fabrication

25VL741	VLSI Fabrication	3	0	0	3
25VL742	Physical Design	3	0	0	3
25VL743	Design for Manufacturability	3	0	0	3
25VL744	Data Structures and Algorithms	3	0	0	3
25VL745	Static Timing Analysis	3	0	0	3
25VL746	Machine learning for VLSI	3	0	0	3
25VL747	MEMS Technology	3	0	0	3
25VL748	VLSI Packaging Technologies and Design	3	0	0	3

Advanced VLSI Architectures

25VL751	VLSI Architectures for Multicore and Heterogeneous Computing	3	0	0	3
25VL752	Reconfigurable Computing	3	0	0	3
25VL753	Network on Chip	3	0	0	3
25VL754	Hardware Software Co-Design	3	0	0	3
25VL755	Embedded Computing and Programming	3	0	0	3
25VL756	Emerging Architectures for Machine Learning	3	0	0	3
25VL757	Cryptography	3	0	0	3
25VL758	Internet of Things	3	0	0	3
25VL759	VLSI Signal Processing	3	0	0	3

25VL601 Semiconductor Device Modelling 3-0-0-3

Course Objectives

- Understand semiconductor fundamentals, pn junctions, and MOS structure behavior.
- Analyze two- and three-terminal MOS devices, focusing on inversion and capacitance.
- Model four-terminal MOS transistors across operating regions with practical effects.
- Study short-channel effects, develop large-signal and non-quasi-static models, and gain an overview of modern semiconductor devices.

Course Outcomes: At the end of the course, the student should be able to

CO1: Explain the physical behavior of intrinsic and extrinsic semiconductors, pn junctions, and MOS structures under various biasing conditions.
CO2: Analyze the characteristics of two- and three-terminal MOS devices and interpret the effects of gate voltage on device behavior.
CO3: Model four-terminal MOS transistors considering different regions of operation, mobility variations, and temperature effects.
CO4: Evaluate short-channel effects and develop models for scaled MOS devices, with an overview of advanced structures including SOI, Double Gate, FinFET, and GAA-FETs.

Skills Acquired: Ability to model and analyze semiconductor devices using physical principles and apply advanced MOSFET models for modern nano-scale device design and simulation.

CO-PO Mapping:

CO/PO	PO1	PO2	PO3	PSO1	PSO2	PSO3
CO 1	-	-	-	3	-	-
CO 2	-	-	-	3	2	-
CO 3	-	-	-	3	3	2
CO 4	-	-	-	3	3	2

Syllabus

Unit 1:

Basics of Semiconductor – Intrinsic and Extrinsic Semiconductors, Equilibrium in absence and presence of Electric Field, Non-Equilibrium and Quasi-Fermi Levels, Charge Density. Electric Field, Potential, Poisson's Equation, Transit Time, Drift and Diffusion current, Contact Potentials, The pn Junction. Overview of the MOS Transistor – Structure, Operation and Characteristics of MOS Transistor. The Two-Terminal MOS Structures – Flatband Voltage, Potential Balance and Charge Balance, Effect of Gate-Body Voltage on Surface Condition, Accumulation and Depletion, Inversion, Small-Signal Capacitance.

Unit 2:

The Three-Terminal MOS Structure – Contacting the Inversion Layer, The Body Effect, Regions of Inversion, A "VCB Control" Point of View, Uses for Three-Terminal MOS Structures.

The Four-Terminal MOS Transistor - Transistor Regions of Operation, Complete All-Region Model, Simplified All-Region Models, Models Based on Quasi-Fermi Potentials, Regions of Inversion in Terms of Terminal Voltages, Strong Inversion, Weak Inversion, Moderate-Inversion and Single-Piece Models, Source-Referenced vs. Body-Referenced Modeling, Effective Mobility, Effect of Extrinsic Source and Drain Series Resistances, Temperature Effects, Breakdown, The p-Channel MOS Transistor, Enhancement-Mode and Depletion-Mode Transistors, Model Parameter Values, Model Accuracy, and Model Comparison.

Unit 3:

Small-Dimension Effects - Carrier Velocity Saturation, Channel Length Modulation, Charge Sharing, Drain-Induced Barrier Lowering, Punchthrough, Combining Several Small-Dimension Effects into One Model, Hot Carrier Effects and Impact Ionization, Velocity Overshoot and Ballistic Operation, Polysilicon Depletion, Quantum Mechanical Effects, DC Gate Current, Junction Leakage, Band-to-Band Tunneling and GIDL, Leakage Currents—Particular Cases, The Quest for Ever-Smaller Devices.

Large-Signal Modeling of MOS Transistor - Quasi-Static Operation, Terminal Currents in Quasi-Static Operation, Evaluation of Intrinsic Charges in Quasi-Static Operation, Transit Time under DC Conditions, Limitations of the Quasi-Static Model, Non-Quasi-Static Modeling, Extrinsic Parasitics.

Overview of Modern Semiconductor Devices – SOI MOSFETs, Multi-gate Gate FETs like - Double Gate, FinFET, Gate All Around FETs (GAA-FETs).

Reference(s)

1. Y. Tsividis and C. McAndrew, *Operation and Modeling of the MOS Transistor*, Oxford University Press, 2011.
2. Donald Neamen, Dhrubes Biswas, *Semiconductor Physics and Devices*, McGraw Hill, 2017.
3. Jerry Fossum and Vishal Trivedi, "*Fundamentals of Ultra thin body MOSFETs and FinFETs*", Cambridge University Press, 2013.
4. Jean-Pierre Colinge "*FinFETs and other Multi Gate Transistors*", Springer (2008).
5. Samar K. Saha, "*Compact Models for Integrated Circuit Design - Conventional Transistors and Beyond*", CRC Press (Taylor & Francis), 2016.

25VL602 CMOS Digital Integrated Circuits 3-0-0-3

Course Objectives

- To introduce the concept of MOS and CMOS logic styles.
- To comprehend the design of transistor level digital circuits.
- To enable learning different logical implementation styles.
- To impart knowledge on switch level RC delay models and data path sub systems.

Course Outcomes: At the end of the course, the student should be able to

CO1: Understand/visualize the digital logic functions at device level.
CO2: Apply suitable CMOS logical styles for the given application.
CO3: Analyze the architecture and characterization of combinational circuits.
CO4: Design digital CMOS circuits, subsystems and measure delay performance.

Skills Acquired: Design of CMOS logic circuits and performance analysis of digital architectures.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	2	2	-	2
CO 2	-	-	2	2	2	2
CO 3	-	-	3	3	3	3
CO 4	-	-	3	3	3	3

Syllabus

Unit 1:

VLSI design flow - NMOS and PMOS Transistors– CMOS Fabrication and Layout - Threshold Voltage - MOS Transistor Theory - I-V and C-V Characteristics - Second-Order Effects - NMOS and CMOS Inverters – Pass Transistors and Transmission Gates - CMOS Combinational Logic Gates

Unit 2:

CMOS Transistor Characteristics - Delay Time Estimation - Switching Characteristics - CMOS Logic Structures – Mirror circuits- Pseudo nMOS logic – Clocked CMOS logic –CPL - Static CMOS Design - Dynamic CMOS Design Charge -Sharing.

Unit 3:

Transistor Sizing - Logical Effort - Scaling - Interconnects – Electros-Static Discharge (ESD) - Latch Up and Prevention – Datapath Subsystems – Addition/Subtraction – Comparators- One/Zero Detectors – Shifters. Sequential Circuit Design (Latches, flip-flops)- RLC Estimation - Elmore's Delay Model.

Reference(s)

1. Neil H. E. Weste and David Money Harris, *CMOS VLSI Design: A Circuits and Systems Perspective*, Fifth Edition, Addison Wesley, 2023.
2. Sung-Mo Kang and Yusuf Leblebici, *CMOS Digital Integrated Circuits - Analysis and Design*, Fourth Edition, Tata McGraw-Hill, 2015.
3. Jan M. Rabaey, Anantha P. Chandrakasan and Borivoje Nikolić, *Digital Integrated Circuits: A Design Perspective*, Second Edition, Prentice Hall India, 2003.

25VL603 Digital Circuits and Systems 3-0-0-3

Course Objectives

- To understand the flow of digital design at the RTL abstraction level with HDL.
- To explore HDL approaches for modeling combinational and sequential circuits

- To introduce design of different subsystems using HDL design flow.

Course Outcomes: At the end of the course, the student should be able to

CO1: Ability to understand the HDL design flow and different modeling styles on hardware synthesis
CO2: Ability to develop systems at the RTL abstraction layer.
CO3: Ability to develop models for combinational and sequential blocks.
CO4: Ability to model and evaluate architectures for digital systems.

Skills Acquired: Design and modeling system-level architectures at the RTL abstraction level, and implementing the design with FPGA resources.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	3	-	--	
CO 2	-	-	3	3	-	
CO 3	-	-	3	3	-	
CO 4	-	-	3	3	3	

Syllabus

Unit 1:

Introduction to VLSI Design Flow and HDLs –Verilog modeling styles – Gate Level – Structural – Dataflow –RTL Abstraction –RTL Design – Design and Synthesis of Logic Circuits with Verilog HDL.

Unit 2:

Sequential Building Blocks - Latch, Flip-flops – Registers - Shift Registers and Digital Counters – Sequential multiplier – Finite State Machines (FSM)– Types of FSM – Design and Implementation – Capabilities and limitations of FSM –Digital Subsystem Design - FIFOs – Memories –Buffers
Fundamental mode model – Flow table – State reduction Races, Cycles and Hazards.

Unit 3:

Case Study of Design and Modeling of a Simple Digital System - Datapath and Controller Design - Programmable Logic Devices - CPLD - FPGA - Verilog Design for FPGA Synthesis – Introduction to High Level Synthesis.

Reference(s)

1. Michael D. Ciletti, *Advanced Digital Design with Verilog HDL*, Second Edition, Pearson Higher Education, 2011.
2. Stephen Brown and Zvonko Vranesic, *Fundamentals of Digital Logic with Verilog Design*, Third Edition, McGraw Hill, 2014.
3. Morris Mano and Michael D. Ciletti, Digital Design: *With an Introduction to the Verilog HDL*, Fifth Edition, Pearson Higher Education, 2013.

4. Peter Minns and Lan Elliott, *FSMBased Digital Design Using Verilog HDL*, Fifth Edition, John Wiley and Sons Ltd, 2008.
5. Scott Hauck and Andre` DeHon, "*Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation*", Morgan Kaufmann, July 2010.
6. Stephen M. Trimberger, *"Field – programmable Gate Array Technology*", Springer, 2007.

25VL604 Analog VLSI Circuits 3-0-0-3

Course Objectives

- To provide an overview of MOS characteristics and its importance in analog design
- To introduce the design and analysis of active loaded amplifiers with and without feedback
- To provide a practical approach for the design of operational amplifiers in nanometer CMOS technology using modern engineering tools

Course Outcomes: At the end of the course, the student should be able to

CO1: Ability to understand MOS characteristics and to design current sources
CO2: Ability to apply techniques to design actively loaded amplifiers with and without feedback
CO3: Ability to design and analyze operational amplifiers, comparators and oscillators
CO4: Ability to analyze amplifier characteristics from top-level specifications and to model circuits using circuit simulators

Skills Acquired: Provides a platform to design and analyze CMOS-based active loaded amplifiers and to verify with the help of industry standard tools

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	3	1	2	1
CO 2	-	-	3	1	2	1
CO 3	-	-	3	-	2	-
CO 4	-	-	3	3	2	1

Syllabus

Unit 1:

MOSFET: Characteristics – Biasing - Large-Signal Equivalent - Small-Signal Operation and Models - High-Frequency Modeling - Short Channel Effects. MOS Diodes - Active Resistors-Capacitors. Current Source: Cascode Current Mirrors - Gain-Boosting - Current and Voltage References - Supply Independent Biasing – Sensitivity.

Unit 2:

Single-Stage MOS Inverters: Active Load - Current Source Load - Push-Pull Load - Small Signal Gain - Frequency Response - Miller Effect-3-dB Frequency Determination. MOS Amplifier Configurations: Common Gate - Common Drain - Cascode - Differential - Active Loaded Differential Pair. Feedback Amplifiers: Negative Feedback - Loop Gain – Oscillators - Comparators.

Unit 3:

Two-Stage CMOS Op-Amp Design: Gain and Frequency Response - Stability and Compensation in CMOS Op-Amps - Miller Compensated Op-Amp - Lead-Lag Compensation. Case Study of CA3130: BiMOS Operational Amplifier with MOSFET Input/CMOS Output.

Reference(s)

1. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Third Edition, Oxford Press, 2011.
2. B. Razavi, *Design of Analog CMOS Integrated Circuits*, Tata McGraw Hill, 2002, Reprint 2015.
3. P. R. Gray, P. J. Hurst, S. H. Levis and R. G. Meyer, *Analysis and Design of Analog Integrated Circuits*, Fifth Edition, Wiley Student Edition, 2009.
4. A S. Sedra, K. C. Smith and A. N. Chandorkar, *Microelectronic Circuits -Theory and Applications*, Seventh Edition, Oxford University Press, 2017.

25VL605 Computer Aided Design for VLSI Circuits 3-0-0-3

Course Objectives

- To introduce physical design cycle.
- To introduce VLSI Design methodologies and provide an understanding of the VLSI design automation tools.
- To emphasize placement, floor planning and routing.
- To provide an understanding of evaluation of combinational logic synthesis.

Course Outcomes: At the end of the course, the student should be able to
CO1: Understand the VLSI physical design cycle
CO2: Apply the VLSI design automation tools
CO3: Analyze placement, floor planning and routing algorithms
CO4: Evaluate combinational logic synthesis.

Skills Acquired: Provide a platform for understanding and applying CAD tools for VLSI physical design.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	3	3	-	2
CO 2	2	-	3	3	2	2
CO 3	2	-	3	3	2	2
CO4	2	-	3	3	3	3

Syllabus

Unit 1:

VLSI Design methodologies- Introduction to VLSI design automation tools-Data structures for the representation of graphs-computational complexity- Graph algorithms - Combinatorial optimization problems-Decision problems - Complexity classes – NP-completeness and NP-hardness

Unit 2:

VLSI Physical Design Cycle - Placement algorithms - Partitioning-Kernighan-Lin partitioning algorithm - Terminology and floor plan representation - Optimization problems in floor planning - Types of local routing problems - Classification of compaction algorithms.

Unit 3:

Combinational Logic Synthesis- Binary Decision Diagrams-hardware models for high level synthesis-Allocation-Assignment and scheduling- scheduling algorithms.

Reference(s)

1. S.H. Gerez, *Algorithms for VLSI Design Automation*, John Wiley & Sons, 2002.
2. N.A. Sherwani, *Algorithms for VLSI Physical Design Automation*, Kluwer Academic Publishers, 2002.
3. Sadiq M. Sait, Habib Youssef, *VLSI Physical Design automation: Theory and Practice*, World Scientific 1999.
4. K. Golshan, *Physical Design Essentials: An ASIC Design Implementation Perspective*, Springer, 2010.
5. M. Sarrafzadeh and C.K. Wong, "An introduction to physical design", McGraw Hill.

25VL681 Analog VLSI and Device Modelling Lab 0-0-3-1

Course Objectives

- To understand MOS characteristics and to design and analysis of active loaded amplifiers in nanometer CMOS technology
- To understand device operation and characteristics through hands-on experiments.
- To simulate and analyze semiconductor devices like diodes, BJTs, MOSFETs, and Junctionless FETs.

Course Outcomes: At the end of the course, the student should be able to

CO1: Ability to understand MOS characteristics and to design current sources
CO2: Ability to apply techniques to design actively loaded amplifiers
CO3: Simulate and analyze the electrical characteristics of semiconductor devices.
CO4: Interpret device behavior and performance metrics under various design and biasing conditions.

Skills Acquired: This lab provides a platform to design and analyze CMOS-based active loaded amplifiers with the help of industry standard tools. Moreover, students will acquire skills for simulating and analyzing semiconductor devices such as diodes, BJTs, MOSFETs, and Junctionless FETs. This helps them to interpret device behavior, evaluate performance metrics, and apply semiconductor physics concepts in virtual device design and provides way for optimization.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	2	3	3	2
CO 2	-	-	3	3	3	1
CO 3	-	-	-	2	3	2
CO 4	-	-	1	3	3	1

Syllabus

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1. For the given bias current, obtain the output and transfer characteristics of a typical 90 nm NMOS device. Determine the effect of varying (i) Drain voltage, (ii) Gate voltage, (iii) Body bias voltage and (iv) Aspect ratio. Repeat for PMOS device
2. Experimentally determine transconductance gain, threshold voltage, overdrive voltage, Early voltage, small signal input-output resistance and voltage gain of the given device for the specified bias point. Based on this, determine (i) Large-signal equivalent, (ii) Small signal equivalent, (iii) High frequency equivalent of the device and (iv)Transit frequency.
3. Construct a common-source amplifier with resistive load by setting the bias point mentioned in Expt. No.1. Based on this, (i) Observe its dc simulation, ac simulation and transient analysis, (ii) Determine the mid-band gain, 3-dB frequency, Gain-bandwidth product, and phase angle from the relevant magnitude and phase plots, (iii) Replace the resistive load by appropriate active load and observe parameters as mentioned in (i) and (ii).
   Note: Active loads may be current source, diode-connected and/or push-pull types
4. Construct an active load differential amplifier by setting the bias point mentioned in Expt. No.1. Based on this, (i)Determine its common-mode gain and differential gain and compute its CMRR and (ii) Observe its linearity and analyze its performance trade-off.
5. Simulation of a PN junction diode to (i) obtain its structure, (ii) obtain diode characteristics, (iii) view contour plots and (iv) extract key device parameters through cutline analysis.
6. Simulation of a BJT to (i) generate the device structure, (ii) study collector current characteristics, (iii) view contour plots and (iv) extract key device parameters through cutline analysis.
7. Simulation of a MOSFET to (i) generate the structure, (ii) analyze drain current for varying drain voltages, (iii) view contour plots and (iv) extract key device parameters through cutline analysis.
8. Simulation of an SOI MOSFET to (i) simulate the device structure, (ii) examine transfer

characteristics, (iii) view contour plots, (iv) extract parameters of short channel effects like Vth, DIBL, Subthreshold slope, ION, IOFF, and ION/ IOFF and (v) extract key device parameters through cutline analysis.

9. Simulation of an SOI Junctionless FET to (i) obtain the structure, (ii) evaluate drain current behavior, (iii) view contour plots, (iv) extract parameters of short channel effects like Vth, DIBL, Subthreshold slope, ION, IOFF, and ION/ IOFF and (v) extract key device parameters through cutline analysis.

Reference(s)

1. B. Razavi, *Design of Analog CMOS Integrated Circuits*, Tata McGraw Hill, 2002, Reprint 2015.
2. P. E. Allen and D. R. Holberg, *CMOS Analog Circuit Design*, Third Edition, Oxford Press, 2011.
3. A S. Sedra, K. C. Smith and A. N. Chandorkar, *Microelectronic Circuits -Theory and Applications*, Seventh Edition, Oxford University Press, 2017.
4. C. K. Sarkar, *Technology Computer Aided Design Simulation for VLSI MOSFET*, 1st Edition, CRC Press, 2013.
5. Silvaco Inc., *Atlas User's Manual*, Device Simulation Software, 2018.

25VL682 RTL Design and FPGA Synthesis Laboratory 0-0-3-1

Course Objectives

- To introduce HDL modeling, verification and simulation at RTL abstraction of combinational and sequential subsystems
- To provide understanding of FPGA Design Flow
- To provide exposure to different HDL modeling styles and their applications
- To instill background in assessing the impact of coding styles on synthesis

Course Outcomes (CO)

CO1: Able to understand modeling styles
CO2: Able to apply modeling styles for realizing digital subsystems
CO3: Able to verify and analyze HDL models by writing appropriate test benches
CO4: Able to realize RTL models on FPGA platforms and evaluate the impact of coding styles on synthesis
CO5: Able to develop RTL architectures for simple digital systems

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	2	3	3	3	2
CO 2	-	2	3	3	3	2
CO 3	-	2	3	3	3	2
CO4	-	2	3	3	3	2
CO5	2	2	3	3	3	2

Syllabus

1 Introduction to HDL simulation flow
2 Structural and Dataflow Modeling in Verilog
3 Behavioral Modeling and Verfication of combinational subsystems
4 Behavioral Modeling, Synthesis and FPGA implementation of combinational subsystems
5 Behavioral Modeling and Verfication of flip-flops, registers and counters
6 Behavioral Modeling and Verification of Finite State Machines
7 Behavioral Modeling, Synthesis and FPGA implementation of flip-flops, registers and counters
8 Behavioral Modeling, Synthesis and FPGA implementation of Finite State Machines
9 Case Study – RTL Architecture, Modeling and Verification of a Complete Digital System
10 Case Study – RTL Architecture Modeling, Synthesis and FPGA Implementation of a Complete Digital System

NB: Scripting exercises with standard tools to be included wherever appropriate.

Recommended Tools: ModelSim, Vivado

Reference(s)

1. Michael D. Ciletti,*Advanced Digital Design with Verilog HDL*, Second Edition, Pearson Higher Education, 2011.
2. Morris Mano and Michael D. Ciletti,*Digital Design: With an Introduction to the Verilog HDL*, Fifth Edition, Pearson Higher Education, 2013.
3. Stephen Brown and Zvonko Vranesic, *Fundamentals of Digital Logic with Verilog Design*, Third Edition, McGraw Hill, 2014
4. Peter Minns and Lan Elliott, *FSM Based Digital Design Using Verilog HDL*, Fifth Edition, John Wiley and Sons Ltd, 2008.
5. Parag K. Lala, *Principles of Modern Digital Design*, Second Edition, John Wiley and Sons Ltd., 2007.

23HU601 Career Competency- I 0-0-3-P/F

Prerequisite:
An open mind and the urge for self-development, basic English language skills and knowledge of high school level arithmetic.

Course Objectives:

- Help students transit from campus to corporate and enhance their soft skills
- Enable students to understand the importance of goal setting and time management skills
- Support them in developing their problem solving and reasoning skills
- Inspire students to enhance their diction, grammar and verbal reasoning skills

Course Outcomes:

CO1: Soft Skills - To develop positive mindset, communicate professionally, manage time effectively and set personal goals and achieve them.
CO2: Soft Skills - To make formal and informal presentations with self-confidence.
CO3: Aptitude - To analyze, understand and employ the most suitable methods to solve questions on arithmetic and algebra.
CO4: Aptitude - To analyze, understand and apply suitable techniques to solve questions on logical reasoning and data analysis.

CO5: Verbal - To infer the meaning of words and use them in the right context. To have a better understanding of the nuances of English grammar and become capable of applying them effectively.

CO6: Verbal - To identify the relationship between words using reasoning skills. To understand and analyze arguments and use inductive/deductive reasoning to arrive at conclusions and communicate ideas/perspectives convincingly.

CO-PO Mapping:

PO/CO	PO1	PO2	PO3
CO1	2	1	-
CO2	2	1	-
CO3	2	1	-
CO4	2	1	-
CO5	1	2	-
CO6	2	2	-

Course content:

Soft Skills:

Introduction to 'campus to corporate transition' -

Communication and listening skills - communication process - barriers to communication - verbal and non-verbal communications - elements of effective communication - listening skills - empathetic listening - role of perception in communication.

Assertiveness skills - the concept - assertiveness and self-esteem - advantages of being assertive - assertiveness and organizational effectiveness.

Self-perception and self-confidence - locus of control (internal v/s external) - person perception - social perception - attribution theories-self presentation and impression management - the concept of self and self-confidence - how to develop self-confidence.

Goal setting - the concept - personal values and personal goals - goal setting theory - six areas of goal setting - process of goal setting - SMART goals - how to set personal goals

Time management - the value of time - setting goals/ planning and prioritizing - check the time killing habits – procrastination - tools for time management - rules for time management - strategies for effective time management

Presentation skills - the process of presentation - adult learning principles - preparation and planning – practice – delivery - effective use of voice and body language - effective use of audiovisual aids - dos and don'ts of effective presentation

Public speaking-an art - language fluency - the domain expertise (Business GK, Current affairs) - self-confidence - the audience - learning principles - body language - energy level and conviction - student presentations in teams of five with debriefing

Verbal:

Vocabulary - Familiarize students with the etymology of words - help them realize the relevance of word analysis and enable them to answer synonym and antonym questions - Create an awareness about the frequently misspelt words - commonly confused words and wrong form of words in English.

Grammar - Train students to understand the nuances of English Grammar and thereby enable them to spot grammatical errors and punctuation errors in sentences.
Reasoning - Stress the importance of understanding the relationship between words through analogy questions and learn logical reasoning through syllogism questions - Emphasize the importance of avoiding the gap (assumption) in arguments/ statements/ communication.
Oral Communication Skills - Aid students in using the gift of the gab to improve their debating skills.
Writing Skills - Introduce formal written communication and keep the students informed about the etiquette of email writing - Make students practice writing emails - especially composing job application emails.

Aptitude:
Numbers - Types - Power Cycles – Divisibility - Prime Factors & Multiples - HCF & LCM - Surds - Indices - Square roots - Cube Roots and Simplification.
Percentage - Basics - Profit - Loss & Discount and Simple & Compound Interest.
Ratio, Proportion & Variation - Basics - Allegations - Mixtures - Partnership.
Averages - Basics - Weighted Average.
Time and Work - Basics - Pipes & Cistern - Work Equivalence.
Time, Speed and Distance - Basics - Average Speed - Relative Speed - Boats & Streams - Races and Circular tracks.
Statistics: -Mean - Median - Mode - Range - Variance - Quartile Deviation - Standard Deviation.
Data Interpretation - Tables - Bar Diagrams - Line Graphs - Pie Charts – Caselets - Mixed Varieties - other forms of data representation.
Equations - Basics - Linear - Quadratic - Equations of Higher Degree - Problems on ages.
Logarithms, Inequalities and Modulus - Basics

Textbooks / References:

Soft Skills:
Communication and listening skills:
[1] Andrew J Durbin, Applied Psychology: Individual and organizational effectiveness, Pearson-Merril Prentice Hall, 2004
[2] Michael G Aamodt, An Applied Approach, 6th edition, Wadsworth Cengage Learning, 2010 Assertiveness skills:
[3] Robert Bolton, Dorothy Grover Bolton, People Style at Word. And Beyond: Making Bad Relationships Good and Good, Ridge Associates Inc., 2009
[4] John Hayes Interpersonal skills at work, Routledge, 2003
[5] Nord, W. R., Brief, A. P., Atieh, J. M., & Doherty, E. M., Meanings of occupational work: A collection of essays (pp. 21- 64), Lexington, MA: Lexington Books, 1990Self-perception and self-confidence:
[6] Mark J Martinko, Attribution theory: an organizational perspective, St. Lucie, 1995
[7] Miles Hewstone, Attribution Theory: Social and Functional Extensions, Blackwell,1983 Time management:
[8] Stephen Covey, The habits of highly effective people, Free press Revised edition, 2004. [online]. Available: https://content.byui.edu/file/3dda7de4-cd79-4390-9bcf-3cb660c48dd1/1/The%207%20Habits%20of%20Highly%20Effective%20People.pdf
[9] Kenneth H Blanchard, The 25 Best Time Management Tools & Techniques: How to Get More Done Without Driving Yourself Crazy, Peak Performance Press, 1st edition 2005
[10] Kenneth H. Blanchard and Spencer Johnson, The One Minute Manager, William Morrow, 1984

Verbal:
[11] Erica Meltzer, The Ultimate Guide to SAT Grammar
[12] Green, Sharon, and Ira K. Wolf, Barron's New GRE, Barron's Educational Series, 2011
[13] Jeff Kolby, Scott Thornburg & Kathleen Pierce, Nova's GRE Prep Course
[14] Kaplan, Kaplan New GRE Premier, 2011-2012
[15] Kaplan's GRE Comprehensive Programme
[16] Lewis Norman, Word Power Made Easy, Goyal Publishers, Reprint edition, 1 June 2011
[17] Manhattan Prep, GRE Verbal Strategies Effective Strategies Practice from 99th Percentile Instructors
[18] Pearson- A Complete Manual for CAT, 2013
[19] R.S. Aggarwal, A Modern Approach to Verbal Reasoning
[20] S. Upendran, Know Your English, Universities Press (India) Limited, 2015
[21] Sharon Weiner Green, Ira K. Wolf, Barron's New GRE, 19th edition (Barron's GRE), 2019
[22] Wren & Martin, English Grammar & Composition
[23] www.bbc.co.uk/learningenglish
[24] www.cambridgeenglish.org
[25] www.englishforeveryone.org
[26] www.merriam-webster.com

Aptitude:
[27] Arun Sharma, How to Prepare for Quantitative Aptitude for the CAT Common Admission Test, Tata Mc Graw Hills, 5th Edition, 2012
[28] Arun Sharma, How to Prepare for Logical Reasoning for the CAT Common Admission Test, Tata Mc Graw Hills, 2nd Edition, 2014
[29] Arun Sharma, How to Prepare for Data Interpretation for the CAT Common Admission Test, Tata Mc Graw Hills, 3rd Edition, 2015
[30] R.S. Aggarwal, Quantitative Aptitude for Competitive Examinations, S. Chand Publishing, 2015. Online. Available: https://eltsindia.com/StudyMaterialFiles/ea007acc-bc55-4e17-8470-0d9e85313252quantitative-aptitude-for-competitive-examinations-by-rs-aggarwal-reprint-2017.pdf
[31] R.S. Aggarwal, A Modern Approach to Verbal & Non-Verbal Reasoning, S. Chand Publishing, Revised-2015. Online. Available: https://vdoc.pub/documents/a-modern-approach-to-verbal-non-verbal-reasoning-3n9dee1ck6p0
[32] Sarvesh Verma, Quantitative Aptitude-Quantum CAT, Arihant Publications, 2016
[33] www.mbatious.com
[34] www.campusgate.co.in
[35] www.careerbless.com

25VL611 Functional Verification with Hardware Description Languages 3-0-0-3

Course Objectives

- To develop a strong foundation in functional verification techniques used in ASIC/FPGA design
- To familiarize with SystemVerilog constructs for building testbenches and verification environments.
- To cultivate skills in assertion-based verification and functional coverage-driven testing

Course Outcomes: At the end of the course, the student should be able to
CO1: Understand the fundamentals of functional verification and its methodologies.

CO2: Design digital modules and corresponding testbenches using SystemVerilog
CO3: Apply effective methodologies to develop effective verification environments
CO4: Evaluate verification completeness using assertion-based techniques.

Skills Acquired: Creation of reusable testbenches using SystemVerilog; Verification planning and coverage closure; Application of functional coverage and assertion-based techniques.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1			3	2		
CO 2			3	3	3	2
CO 3			3	3	3	3
CO 4			3	3	2	2

Syllabus

Unit 1:

Review of HDL (Verilog) –Need for functional verification - Verification lifecycle and test planning - Testbench architectures: Directed & Constraint Random - Types of coverage: Code coverage - Functional coverage - SystemVerilog for design: data types, control flow, operators - Hierarchy, modules, and connectivity

Unit 2:

SystemVerilog for Verification- Testbench components: tasks, functions, interfaces- Object-oriented features in SystemVerilog (classes, inheritance, polymorphism) - Constrained Random Verification-
Inter Process Communication: Threads, mailboxes and semaphores- Building verification environment with SystemVerilog

Unit 3:

System Verilog Assertions – immediate assertions – concurrent assertions – Boolean assertions - Sequences – properties - implication operators – nested implications – Functional Coverage: covergroups, bins, cross coverage - Coverage closure strategies and reporting – Memory Design: Behavioural Modelling and Verification environment creation – UVM – Overview, Testbench Architecture, and Component Roles

Reference(s)

1. Chris Spear and Greg Tumbush*: SystemVerilog for Verification: A Guide to Learning the Testbench Language Features*, 4th Edition, 2020.
2. Ashok B. Mehta, *Introduction to SystemVerilog: Simulation and Testbench Design*, Springer, 2021.
3. Janick Bergeron, *Writing Testbenches Using SystemVerilog*, 3rd Edition, Springer, 2016.
4. Ben Cohen, Srinivasan Venkataramanan, Ajeetha Kumari, Lisa Piper, *SystemVerilog Assertions Handbook: For Design and Verification*, 4th Edition, 2019.

25VL612 Digital VLSI Testing & Testability 3-0-2-4

Course Objectives

- To introduce the fundamentals of VLSI testing and testability.
- To impart knowledge in the development of ATPG algorithms for testing.
- To explore the concepts of DFT and BIST.

Course Outcomes: At the end of the course, the student should be able to
CO1: Ability to understand the concept of testing and testability in VLSI circuits.
CO2: Ability to apply test pattern generation algorithms.
CO3: Ability to analyze built-in-test concepts.
CO4: Ability to design techniques for testability in scan-based architectures

Skills Acquired: Development of testing algorithms and testable scan architectures.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	2	-	2	2
CO 2	-	-	3	3	3	2
CO 3	-	-	3	2	3	2
CO 4	-	-	3	3	3	2

Syllabus

Unit 1:

Concepts of VLSI Circuit Testing - Fault Modeling - Fault Collapsing - True Value Simulation - Fault Simulation - SCOAP Testability Measures - Combinational Circuit Test Generation - Roth's D Algorithm - PODEM ATPG Algorithms.

Unit 2:

Sequential Circuit Test Generation – Simulation based ATPG - Test Set Compaction - NDetect ATPG - Design for Testability - Ad Hoc Techniques - Level-Sensitive Scan Design - Scan Architectures and Testing - Scan Design Rules - LFSR based Testing.

Unit 3:

Testable Logic Circuit Design - Logic BIST Architectures - Test Pattern Generation – Output Response Analysis - Test Stimulus Compression - Test Response Compaction - Memory BIST – RAM fault models - RAM Test Generation - Boundary Scan Architecture.

List of Experiments:
1. Algorithms for fault list reduction
2. Algorithms for test pattern generation

3. Algorithms for fault simulation
4. Algorithms for computing SCOAP Testability Measures
5. Algorithms for test power reduction
6. A script to automate T-max tool flow in Synopsys

Reference(s)

1. Vishwani D. Agrawal and Michael L. Bushnell, *Essentials of Electronic Testing for Digital Memory and Mixed Signal VLSI Circuits*, Kluwer Academic Publishers, 2000.
2. Parag K. Lala, *An Introduction to Logic Circuit Testing*, Morgan &Claypool Publishers, 2009.
3. L. T. Wang, Cheng Wen Wu and Xiaoqing Wen, *VLSI Test Principles and Architectures Design for Testability*, First Edition, Morgan Kaufmann Publishers, 2006.
4. Miron Abramovici, Melvin A. Breuer and Arthur D. Friedman, *Digital Systems Testing and Testable Design*, Jaico Publishing House, 2001.

25VL683 ASIC Frontend and Backend lab 0-0-3-1

Course Outcomes: At the end of the course, the student should be able to
CO1: To gain understanding of the detailed steps involved in FE and BE.
CO2: Design ASIC based digital systems using industry standard EDA tools
CO3: Design, simulate and synthesize complex digital system

Skills Acquired:

- ASIC based system designs using EDA tools
- Design and synthesis of complex digital systems

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1		2	3	3	3	
CO 2		2	2	3	3	
CO 3		2	2	3	3	
CO 4		2	3	3	3	

Syllabus

A suitable low complex CUT can be considered for the entire flow.

ASIC Frontend Flow Lab Experiments

1. Design of Digital Architecture for given specification (Verilog/System Verilog based RTL coding and simulation of combinational and finite state machine based design)
2. Logical Synthesis of Digital Architecture (RTL to Gate level Netlist)
3. Functional Verification (System Verilog based TB development)
4. Static timing Analysis (STA) (set up/hold violation. Critical path analysis, Clock skew and uncertainty)

ASIC Backend Flow Lab Experiments

5. Floor planning (Floor plan layout files, Placement of macros, Pin Assignment. Power ring creation)
6. Placement and Clock Tree Synthesis (Placement optimization, Clock tree design, skew and latency reduction)
7. Routing (Routing congestion, and optimization, Later assignments and via usage, Routing DRC)
8. Post layout Verification (DRC and LVS Check).
9. Power planning and IR Drop (Power mess creation, IR drop distribution)
10. Parasitic Extraction and Post Layout STA (parasitic modelling, crosstalk and signal integrity, reverification after layout).

Reference(s)

1. Farzad Nekoogar, Faranak Nekoogar, "*From ASICs to SOCs: A Practical Approach",* Pearson, 2003.
2. Luciano Lavagno, Louis Scheffer, and Grant Martin. *EDA for IC Implementation, Circuit Design, and ProcessTechnology (Electronic Design Automation for Integrated Circuits Handbook)*. CRC Press, Inc., USA, 2006.
3. EDA manuals from Synopsys and Cadence
4. Stuart Sutherland, "*RTL Modeling With System Verilog for Simulation and Synthesis: Using System Verilog for ASIC and FPGA Design*", Sutherland HDL Inc., 2017
5. Naveed Sherwani, "*Algorithms for VLSI Physical Design Automation*", Kluwer Academic Publishers in 1993.

25VL684 Functional Verification Lab 0-0-3-1

Course Objectives

- To provide hands-on experience in functional verification of RTL designs using SystemVerilog.
- To develop skills in object-oriented programming and constrained random verification
- To create scalable verification environments using SystemVerilog interfaces,

Course Outcomes: At the end of the course, the student should be able to
CO1: Understand SystemVerilog RTL modeling and verification constructs
CO2: Apply object-oriented programming to create reusable testbench components

CO3: Analyze and verify DUT functionality using constrained random stimulus and interprocess communication techniques.
CO4: Design and implement complete testbenches using interface-based and layered architecture

Skills Acquired:

- Design and verification of RTL modules in SystemVerilog
- Development of class-based testbenches using OOP

- Exposure to practical industry-standard verification flow

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1		2	3	3	3	
CO 2		2	2	3	3	
CO 3		2	2	3	3	
CO 4		2	3	3	3	2

Syllabus

1 RTL Modeling of Combinational Circuits using SystemVerilog
2 RTL Modeling of Sequential Circuits using SystemVerilog
3 Exploration of SystemVerilog Data Types and Constructs
4 Design and use of interface for Structured Connectivity
5 Introduction to Classes and Basic Object-Oriented Programming
6 Advanced OOP in SystemVerilog: Inheritance and Polymorphism
7 Concurrency and Inter-Process Communication: Mailboxes and Semaphores
8 Building a Layered Testbench for an Adder/Memory – Basic Driver and Stimulus
9 Layered Testbench with Monitors, Reference Models, and Scoreboards
10 Adding Assertions and Functional Coverage to SystemVerilog Testbench
11 Introduction to UVM: Testbench Architecture, Components, and Execution Flow
12 Hands-On UVM Lab: Building a Minimal UVM Testbench for a 4-bit Counter

NB: Scripting exercises with standard tools to be included wherever appropriate.

Reference(s)

1. Chris Spear and Greg Tumbush*: SystemVerilog for Verification: A Guide to Learning the Testbench Language Features* (4th Edition, 2020).
2. Ashok B. Mehta, *Introduction to SystemVerilog: Simulation and Testbench Design* (Springer, 2021).
3. Janick Bergeron, *Writing Testbenches Using SystemVerilog* (3rd Edition, Springer, 2016).
4. Ben Cohen, Srinivasan Venkataramanan, Ajeetha Kumari, Lisa Piper, *SystemVerilog Assertions Handbook: For Design and Verification* (4th Edition, 2019).

25RM604 Research Methodology 2-0-0-2

Course Objectives

- To enable defining and formulating research approaches towards obtaining solutions to practical problems.
- To facilitate development of scientific oral and written communication skills.
- To comprehend the concepts behind adhering to scientific ethics and values.

Course Outcomes : At the end of the course, the student should be able to

CO1: Ability to understand some basic concepts of research and its methodologies.
CO2: Ability to define and apply appropriate parameters and research problems.
CO3: Ability to develop skills to draft a research paper.
CO4: Ability to analyse and comprehend the ethical practices in conducting research and dissemination of results in different forms.

Skills Acquired: Design, analyse and conduct research and comprehend the results.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	2	3	3	2	3	3
CO 2	2	3	3	2	3	3
CO 3	2	3	3	2	3	3
CO 4	2	3	3	2	3	3

Syllabus

Meaning of Research, Types of Research, Research Process, Problem definition, Objectives of Research, Research Questions, Research design, Approaches to Research, Quantitative vs. Qualitative Approach, Understanding Theory, Building and Validating Theoretical Models, Exploratory vs. Confirmatory Research, Experimental vs Theoretical Research, Importance of reasoning in research. Problem Formulation, Understanding Modeling & Simulation, Conducting Literature Review, Referencing, Information Sources, Information Retrieval, Role of libraries in Information Retrieval, Tools for identifying literatures, Indexing and abstracting services, Citation indexes Experimental

Research: Cause effect relationship, Development of Hypothesis, Measurement Systems Analysis, Error Propagation, Validity of experiments, Statistical Design of Experiments, Field Experiments, Data/Variable Types & Classification, Data collection, Numerical and Graphical Data Analysis:

Sampling, Observation, Surveys, Inferential Statistics, and Interpretation of Results Preparation of Dissertation and Research Papers, Tables and illustrations, Guidelines for writing the abstract, introduction, methodology, results and discussion, conclusion sections of a manuscript. References, Citation and listing system of documents Intellectual property rights (IPR) - patents-copyrights- Trademarks-Industrial design geographical indication. Ethics of Research- Scientific

Misconduct- Forms of Scientific Misconduct. Plagiarism, Unscientific practices in thesis work, Ethics in science.

Reference(s)

1. Bordens, K. S. and Abbott, B. B., *Research Design and Methods – A Process Approach*, 8th Edition, McGraw-Hill, 2011.
2. C. R. Kothari, *Research Methodology – Methods and Techniques*, 2nd Edition, New Age International Publishers.
3. Davis, M., Davis K., and Dunagan M., *Scientific Papers and Presentations*, 3rdEdition, Elsevier Inc.
4. Michael P. Marder, *Research Methods for Science*, Cambridge University Press, 2011.
5. T. Ramappa, *Intellectual Property Rights Under WTO*, S. Chand, 2008.
6. Robert P. Merges, Peter S. Menell, Mark A. Lemley, *Intellectual Property in New Technological Age, Aspen Law & Business*, 6th Edition July 2012.
7. Tony Greenfield and Sue Greener, *Research Methods for Postgraduates*, 3rd Edition, John Wiley & Sons Ltd., 2016

23HU611 Career Competency II 0-0-3-1

Pre-Requisite:
Willingness to learn, team spirit, basic English language and communication skills and knowledge of high school level arithmetic.

Course Objectives:

- Help students to understand the importance of interpersonal skills and teamwork
- Prepare the students for effective group discussions and interviews participation.
- Help students to sharpen their problem solving and reasoning skills
- Empower students to communicate effectively by using the correct diction, grammar and verbal reasoning skills

Course Outcomes:

CO1: To demonstrate good interpersonal skills, solve problems and effectively participate in group discussions.
CO2: To write technical resume and perform effectively in interviews.
CO3: To identify, investigate and arrive at appropriate strategies to solve questions on arithmetic by managing time effectively.
CO4: To investigate, understand and use appropriate techniques to solve questions on logical reasoning and data analysis by managing time effectively.
C05: To be able to use diction that is more refined and appropriate and to be competent in knowledge of grammar to correct/improve sentences
C06: To be able to examine, interpret and investigate passages and to be able to generate ideas, structure them logically and express them in a style that is comprehensible to the audience/recipient.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3
CO 1	2	2	1
CO 2	2	2	1
CO 3	2	2	1
CO 4	2	2	1
CO 5	1	1	2
CO 6	2	2	2

Course contents:

Soft Skills:

Interpersonal skill - Ability to manage conflict – flexibility - empathetic listening - assertiveness - stress management - problem solving - understanding one's own interpersonal needs - role of effective teamwork in organizations - Group problem solving: the process - the challenges - the skills and knowledge required for the same.
Conflict management - the concept - its impact and importance in personal and professional lives (activity to identify personal style of conflict management - developing insights that help in future conflict management situations.)
Team building and working effectively in teams - the concept of groups (teams) - different stages of group formation - process of team building - group dynamics - characteristics of effective team - role of leadership in team effectiveness - (Exercise to demonstrate the process of emergence of leadership in a group, debrief and reflection) - group discussions.
Interview skills - what is the purpose of a job interview - types of job interviews - how to prepare for an interview, dos and don'ts of interview - One on one mock interview sessions with each student

Verbal:

Vocabulary - Help students understand the usage of words in different contexts. Stress the importance of using refined language through idioms and phrasal verbs.
Grammar - Enable students to identify poorly constructed sentences or incorrect sentences and improvise or correct them.
Reasoning - Facilitate the student to tap her/his reasoning skills through critical reasoning questions and logical ordering of sentences.
Reading Comprehension - Enlighten students on the different strategies involved in tackling reading comprehension questions.
Public Speaking Skills - Empower students to overcome glossophobia and speak effectively and confidently before an audience.
Writing Skills - Practice closet tests that assess basic knowledge and skills in usage and mechanics of writing such as punctuation, basic grammar and usage, sentence structure and rhetorical skills such as writing strategy, organization, and style.

Aptitude:

Sequence and Series: Basics, AP, GP, HP, and Special Series.

Geometry: 2D, 3D, Coordinate Geometry, Heights & Distance.

Permutations & Combinations: Basics, Fundamental Counting Principle, Circular Arrangements, and Derangements.
Probability: Basics, Addition & Multiplication Theorems, Conditional Probability and Bayes' Theorem. **Logical Reasoning:** Arrangements, Sequencing, Scheduling, Venn Diagram, Network Diagrams, Binary Logic, and Logical Connectives, Clocks, Calendars, Cubes, Non-Verbal reasoning and Symbol based reasoning.
Logical Reasoning II: Blood Relations, Direction Test, Syllogisms, Series, Odd man out, Coding & Decoding, Cryptarithmetic Problems and Input - Output Reasoning.
Data Sufficiency: Introduction, 5 Options Data Sufficiency and 4 Options Data Sufficiency.
Campus recruitment papers: Discussion of previous year's question papers of all major recruiters of Amrita Vishwa Vidyapeetham.

Miscellaneous: Interview Puzzles, Calculation Techniques and Time Management Strategies.

Textbooks / References:

Soft Skills:

Team Building:

[1] Thomas L. Quick, Successful team building, AMACOM Div American Mgmt Assn, 1992
[2] Brian Cole Miller, Quick Team-Building Activities for Busy Managers: 50 Exercises That Get Results in Just 15 Minutes, AMACOM; 1 edition, 2003.
[3] Patrick Lencioni, The Five Dysfunctions of a Team: A Leadership Fable, Jossey-Bass, 1st Edition, 2002

Verbal:

[4] GMAT Official Guide by the Graduate Management Admission Council, 2019
[5] Arun Sharma, How to Prepare for Verbal Ability and Reading Comprehension For CAT
[6] Joern Meissner, Turbocharge Your GMAT Sentence Correction Study Guide, 2012
[7] Kaplan, Kaplan GMAT 2012 & 13
[8] Kaplan, New GMAT Premier, Kaplan Publishing, U.K., 2013
[9] Manhattan Prep, Critical Reasoning 6th Edition GMAT
[10] Manhattan Prep, Sentence Correction 6th Edition GMAT
[11] Mike Barrett SAT Prep Black Book the Most Effective SAT Strategies Ever Published
[12] Mike Bryon, Verbal Reasoning Test Workbook Unbeatable Practice for Verbal Ability, English Usage and Interpretation and Judgement Tests
[13] www.bristol.ac.uk/arts/skills/grammar/grammar_tutorial/page_55.htm
[14] www.campusgate.co.in

Aptitude:

[15] Arun Sharma, How to Prepare for Quantitative Aptitude for the CAT Common Admission Test, Tata Mc Graw Hills, 5th Edition, 2012
[16] Arun Sharma, How to Prepare for Logical Reasoning for the CAT Common Admission Test, Tata Mc Graw Hills, 2nd Edition, 2014
[17] Arun Sharma, How to Prepare for Data Interpretation for the CAT Common Admission Test, Tata Mc Graw Hills, 3rd Edition, 2015
[18] R.S. Aggarwal, Quantitative Aptitude for Competitive Examinations, S. Chand Publishing, 2015
[19] R.S. Aggarwal, A Modern Approach to Verbal & Non-Verbal Reasoning, S. Chand Publishing, Revised -2015
[20] Sarvesh Verma, Quantitative Aptitude-Quantum CAT, Arihant Publications, 2016
[21] www.mbatious.com

[22] www.campusgate.co.in
[23] www.careerbless.com

25VL698 Industry Internship 0-0-2-1

Course Objectives:

- To expose the students to industry setting and get acquainted with its various functions.
- To gain direct experience so as to relate and reinforce the concepts learned in the class room
- To promote collaboration between industry/Research Laboratory and the institution

Course Outcomes

CO1: Familiarize with the industry environment/Research Laboratory
CO2: Understand the application of theoretical concepts in a practical setting.
CO3: Prepare technical documents/presentations related to the work completed

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	3	2	3	3
CO 2	-	-	3	2	3	3
CO 3	-	3	3	2	3	3

Syllabus

Students have to undergo practical training in VLSI or allied industries/research laboratory of their choice with the approval of the department. At the end of the training student should submit a report and certificate of completion to the department in the prescribed format.

25VL798 Dissertation Phase I 0-0-30-10

Course Objectives

- To enhance students' ability to conduct independent research, including literature review, data collection, and analysis.
- To foster critical analysis of existing literature and methodologies in the chosen field of study.
- To gain proficiency in selecting appropriate research methods and techniques for addressing research questions.

Course Outcomes: At the end of the course, the student should be able to

CO1: Ability to define a research problem.
CO2: Ability to apply engineering concepts to the research problem.
CO3: Ability to design and conduct independent research in the domain of interest.
CO4: Ability to evaluate and analyze the outcomes of the research.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	2	3	3	2	3	3
CO 2	2	3	3	2	3	3
CO 3	2	3	3	2	3	3
CO 4	2	3	3	2	3	3

Syllabus

Problems and concepts may be defined based on extensive literature survey by standard research articles. Significance of proposed problem and the state-of the art to be explored. Industry relevant tools may be used for demonstrating the results with physical meaning and create necessary research components. Publications in reputed journals /conferences may be considered for authenticating the results. Prepare and submit a detailed technical report. Provide a presentation and defend the dissertation work carried out.

25VL799 Dissertation Phase II 0-0-45-15

Course Objectives

- To enhance students' ability to conduct independent research, including literature review, data collection, and analysis.
- To foster critical analysis of existing literature and methodologies in the chosen field of study.
- To gain proficiency in selecting appropriate research methods and techniques for addressing research questions.

Course Outcomes: At the end of the course, the student should be able to

CO1: Ability to define a research problem.
CO2: Ability to apply engineering concepts to the research problem.
CO3: Ability to design and conduct independent research in the domain of interest.
CO4: Ability to evaluate and analyze the outcomes of the research

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	2	3	3	2	3	3
CO 2	2	3	3	2	3	3
CO 3	2	3	3	2	3	3
CO 4	2	3	3	2	3	3

Syllabus:

Problems and concepts may be defined based on extensive literature survey by standard research articles. Significance of proposed problem and the state-of the art to be explored. Industry relevant tools may be used for demonstrating the results with physical meaning and create necessary research components. Publications in reputed journals /conferences may be considered for authenticating the results. Prepare and submit a detailed technical report. Provide a presentation and defend the dissertation work carried out.

25VL731 Semiconductor Memory Design 3-0-0-3

Course Objectives

- To understand the architecture, operation, and applications of various semiconductor memory technologies, including SRAM, DRAM, ROM, PROM, EPROM, EEPROM, and Flash memory.
- To explore advanced memory technologies such as FRAM, MRAM, and GaAs- based memories, along with their advantages and applications.
- To study emerging memory technologies, including experimental memory devices, and their potential impact on future semiconductor memory design.
- To analyze and compare different memory architectures to optimize performance and power consumption for specific applications.

Course Outcomes: At the end of the course, the student should be able to

CO1**:** understand the fundamental principles and working mechanisms of various memory technologies, including SRAM, DRAM, and nonvolatile memories.

CO2**:** compare advanced memory technologies such as FRAM, MRAM, and experimental memory devices for their advantages and limitations.

CO3**:** analyze different memory architectures and their applications in modern computing systems.

CO4**:** apply knowledge of memory technologies to design and optimize memory systems for specific applications.

Skills Acquired: The student will acquire the ability to understand and differentiate various memory technologies, analyze memory architectures and their impact on system performance, evaluate emerging memory technologies for advanced applications, and apply memory design concepts for optimization in real-world scenarios.

CO-PO Mapping:

CO/PO	PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	-	-	3	3	-	-
CO2	-	-	3	3	-	-
CO3	-	-	3	2	-	-
CO4	-	-	3	3	-	2

Syllabus

Unit 1:

Static Random-Access Memories (SRAMs): SRAM cell structure, MOS SRAM architectures, MOS RAM Cell and Peripheral circuit operation, Bipolar SRAM technologies, Silicon on Insulator (SOI) Technology, Advanced SRAM architectures, Application-specific SRAMs.

Dynamic Random-Access Memories (DRAMs): DRAM technology development, CMOS DRAMs, DRAM Cell Theory and Advanced cell structures, BiCMOS DRAMs, Soft-Error

failures in DRAMs, Advanced DRAM Designs and Architectures, Application-Specific DRAMs.

Unit 2:

Read-Only Memories (ROMs): Masked ROMs, Technology development and Cell programming, High-Density (Multimegabit) ROMs. Programmable Read-Only Memories (PROMs): Bipolar PROMs, CMOS PROMs. Erasable (UV) Programmable Read-Only Memories (EPROMs): Floating-gate EPROM cells, EPROM Technology Developments, Advanced EPROM Architectures, One-Time Programmable (OTP) EPROMs.

Electrically Erasable PROMs (EEPROMs): EEPROM technologies – MNOS, SONOS, FLOTOX, Textured-Polysilicon Technology; EEPROM architectures, nonvolatile SRAM (Shadow RAM). Flash Memories: Flash memory cells and Technology Developments, Advanced Flash Memory Architectures.

Unit 3:

Ferroelectric Random-Access Memories (FRAMs): Basic theory, FRAM Cell and Memory Operation, FRAM Technology Developments, comparison of FRAMs with EEPROMs.Gallium Arsenide (GaAs) FRAMs: GaAs-based FRAM technologies and applications. Analog Memories: Concepts and applications of analog memory technologies. Magnetoresistive Random Access Memories (MRAMs): MRAM technology and advancements.

Experimental Memory Devices: Quantum-Mechanical Switch Memories, GaAs n-p-n-p Thyristor/JFET Memory cell, Single-Electron Memory, Neuron-MOS Multiple-Valued (MV) Memory Technology.

Reference(s)

1. Ashok K.Sharma, *Semiconductor Memories Technology, testing and reliability*, Prentice hall of India Private Limited, New Delhi 1997.
2. Ashok K Sharma, *Advanced Semiconductor Memories – Architecture, Design and Applications*, Wiley 2002.
3. Shimeng Yu, *Semiconductor Memory Devices and Circuits*, CRC Press, 2013.

25VL732 Mixed Signal VLSI Design 3-0-0-3

Course Objectives

- To introduce the concepts of mixed signal VLSI circuits
- To enhance design thinking capability by inculcating the importance of parameters like non-linearity, mismatches, noise and jitter in mixed signal circuit design
- To enrich the skills of computations by providing practical design problems and to make them solve using modern engineering tools involving nanometer CMOS technology

Course Outcomes: At the end of the course, the student should be able to

CO1: Ability to apply the concepts of mixed signal processing and to understand the working of mixed signal circuits

CO2: Ability to apply amplifier basics to design integrators, filters and switched capacitance circuits

CO3: Ability to analyze non-linearity, mismatches, noise and jitters in mixed signal circuits

CO4: Ability to analyze mixed signal designs from top-level specifications and to model circuits using Verilog-AMS

Skills Acquired: To become skilled in designing CMOS-based mixed signal functional blocks and to expertise in using high-level descriptive languages

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	1	-	-	-
CO 2	-	-	3	1	2	1
CO 3	-	-	3	-	-	-
CO 4	-	-	3	1	2	1

Syllabus

Unit 1:

Sampling Theory - Spectral Properties of Sampled Signals - Oversampling -. Time Interleaved Sampling - Ping-Pong Sampling System - Analysis of Offset and Gain Errors - Discrete Time Signals - Sample and Hold Circuits: Top and Bottom Plate Sampling- Characterizing Sample and Hold - Choice of Input Frequency. Anti-Alias Filter Design:

Integrator-Based Filter - The gm-C Filter - Discrete Time Integrators - Filtering Topologies - Filters Using Noise Shaping. Verilog-A Modeling of Filters.

Unit 2:

Switched Capacitor Circuits: Capacitors - Switches - Non-Overlapping Clocks - Resistor Equivalence - Parasitic Sensitive Integrator - Parasitic - Insensitive Integrators - Parasitic Insensitive Switched Capacitor Amplifiers - Non-Idealities - Finite Gain - DC Offset - Gain Bandwidth Product - Fully Differential Switched Capacitor Circuits - Noise - Applications of Switched Capacitor Circuits. Overview of sigma-delta ADC. Verilog-A Modeling of Switched Capacitor Circuits.

Unit 3:

Basic Phase-Locked Loop (PLL) Architecture: Voltage Controlled Oscillator (VCO) - Analog Phase Detector - Digital Phase Detector - Loop Filer - Dynamics of Simple PLL – Charge-Pump PLL - Dynamics of Charge-Pump PLL – Nonideal Effects in PLL - Jitter and Phase Noise – Overview of PLL Applications– Clock Generation - Jitter Reduction. RC Phase Shift - LC Oscillators – Negative-gm Oscillators. Verilog-A Modeling: VCO - Phase Detectors - Loop Filters –Simple PLL - Charge-pump PLL.

Reference(s):

1. R. Jacob Baker, *CMOS Mixed Signal Circuit Design*, Wiley India Pvt. Ltd, 2008.
2. B. Razavi, *Design of Analog CMOS Integrated Circuits*, Tata McGraw Hill, 2002, Reprint 2015.
3. R.Gregorian and G.C.Temes, *Analog MOS Integrated Circuits for Signal Processing*, John Wiley and Sons, 2004.
4. David A. Johns and Ken Martin, *Analog Integrated Circuit Design*, Wiley India Pvt. Ltd, 2008.
5. Kenneth S. Kundart and Olaf Zinke, *The Designer's Guide to Verilog- AMS*, Springer, 2004.
6. Haykin, Simon, and Barry Van Veen. *Signals and systems*. John Wiley & Sons, 2007.
7. A S. Sedra, K. C. Smith and A. N. Chandorkar, *Microelectronic Circuits -Theory and Applications*, Seventh Edition, Oxford University Press, 2017.

25VL733 CMOS RF IC Design 3-0-0-3

Course Objectives

- To provide an overview of RF CMOS device characterization
- To enhance design skills by using two-port network parameters such as MAG/MSG, noise figure, stability, linearity and reflection coefficients in RF ICs
- To gain computation skills and to become an expert in designing RF amplifiers in nanometer CMOS technology using modern engineering tools

Course Outcomes: At the end of the course, the student should be able to
CO1: Ability to understand RF CMOS device characteristics and its importance in RF ICs
CO2: Ability to apply RF computational techniques to design actively loaded RF amplifiers
CO3: Ability to analyze two port network parameters like Forward Gain, Noise Figure, Stability, Linearity, Mismatches and Reflection Coefficients in CMOS-based RF sub-blocks
CO4: Ability to analyze the characteristics of CMOS-based RF sub-blocks from top-level specifications and to model circuits using circuit simulators

Skills Acquired: Provides a platform to design and analyze RF CMOS amplifiers and to verify with the help of industry standard tools

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	2	1	2	1
CO 2	-	-	3	1	2	-
CO 3	-	-	3	-	2	-
CO 4	-	-	3	3	2	1

Syllabus

Unit 1:

Passive RLC Networks: Parallel - Series - Impedance Transformers - L-Pi-T-Type - Higher Order Matching. Circuit Models: Lumped and Distributed Elements - Transmission Lines - Driving Point Impedance - Artificial Lines - Microstrip -CPW. Small Signal RF CMOS Model: Noise Sources - Distributed Gate Effects - Multi-Fingered Gate - Maximum Available Power Gain - Unity Power Gain Frequency.

Unit 2:

Two Port Network: S-Parameters – Maximum Stable Gain - Reflection Coefficients - Stability - Non-Linearity - 1-dB Gain Compression Point - IIP3/OIP3 – Dynamic Range. RF Transmitter: Bit Error Rate - Signal to Noise Ratio - Sensitivity - Receiver Architecture - Direct Conversion - Super Heterodyne - Hartley Architecture. CMOS-based sub-blocks: Low Noise Amplifier - Input Impedance Matching – Topology Classification – Active loads - Inductive Source Degeneration - Cascode and Differential Configurations - Inductive Peaking - Current Reuse.

Unit 3:

High Frequency Amplifier Design: Bandwidth Enhancement - Tuned Amplifiers - Broadband Monolithic Distributed Amplifier. Mixer Fundamentals: Nonlinear Systems as Linear Mixers – CMOS-Based Down-Conversion Mixers - Single-Balanced - Double Balanced Gilbert Cell Mixer. CMOS-Based Power Amplifiers: Classification - Doherty Power Amplifiers. Case Study of ADAR2004: 10 GHz to 40 GHz, 4-Channel Rx Mixer with 4× LO Multiplier/Filter.

Reference(s):

1. Thomas H. Lee, *The Design of CMOS Radio Frequency Integrated Circuits,* Second Edition, Cambridge University Press, 2004, Indian Reprint of 2009.
2. SorinVoinigescu, *High-Frequency Integrated Circuits,* Cambridge University Press, 2013, South Asian Paperback edition of 2018.
3. B. Razavi, *RF Microelectronics*, Second Edition, Pearson, 2012 (Indian Edition 2013 by Dorling Kindersley).
4. Michael Steer, *Microwave and RF Design - A Systems Approach,* SciTech Publishing, 2010, Indian Reprint by Yesdee Publishing, 2012.
5. Mike Golio, ed. *RF and microwave semiconductor device handbook*. CRC press, 2017.

25VL734 FPGA based System Design 3-0-0-3

Course Objectives

- To introduce the internal architecture of programmable logic with focus on FPGA.
- To provide knowledge in FPGA design flow at the architectural and system design.
- To impart a good background in block-based design using standard system level tools.

Course Outcomes: At the end of the course, the student should be able to

CO1: Understand the structure of the fabric of programmable logic.
CO2: Apply techniques for logic designing using field programmable devices.
CO3: Analyze and comprehend FPGA design flow and related design, synthesis, and timing issues.

CO4: Evaluate system level architectures by integrating IP cores, including softcore and hardcore processors.

Skills Acquired: Provide a practical approach for design of embedded systems using FPGAs.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	3	-	-	-
CO 2	2	-	3	-	-	-
CO 3	2	-	3	3	-	-
CO 4	2	-	3	3	-	2

Syllabus

Unit 1:

Programmable Logic Devices - PROM - PAL - PLA - CPLD - Gate Arrays - MPGA - PGA - Programming Technologies - EPROM - EEPROM - FLASH - SRAM - FPGA Fabric - Configurable Logic Block - LUT - Slice - Slicem - Programmable Interconnects - Input Output Blocks - Keeper Circuit - Xilinx 7 Series Architecture.

Unit 2:

FPGA Design Flow and Abstraction Levels - Verilog Design for Synthesis - One Hot Encoding - Memory Blocks - Block Memory Generator (BRAM/BROM) - Single Port Memory - Dual Port Memory - FIFO - Distributed RAM - Synthesis Pitfalls - Latch Inference - Static Timing Analysis - Speed Performance - Timing Constraints - Clock Management - Clock Buffers - Clock Tree Routing.

Unit 3:

Introduction to SoC Design - Hard Macros - Multipliers - DSP Block - Hard Core Processors - Interface Circuits - Configuration Chain - JTAG Interface - Zynq7000 Architecture.

Reference(s)

1. Amano, Hideharu, *Principles and Structures of FPGAs*, First Edition, Springer, 2018.
2. Readler, Blaine C., *Verilog by example: a concise introduction for FPGA design*, Full Arc Press, 2011.
3. ZainalabedinNavabi, *Embedded Core Design with FPGAs, First Edition*, McGraw Hill, 2008.
4. Xilinx Inc, Vivado Design Suite User Guide, 2021.

25VL735 Electronic System Level Design 3-0-0-3

Course Objectives

- To introduce design and verification at system level.
- To introduce Open Source language based design and debug.
- To provide basics of Transaction Level Modelling and High Level Synthesis.
- To introduce portable test and stimulus standards.

Course Outcomes: At the end of the course, the student should be able to
CO1: To Understand Electronic System level Design and Verification.
CO2: Apply system level design methodologies using open-source languages.
CO3: Analyze virtual prototyping and its advantages
CO4: Evaluating the transaction level models built using SystemC.

Skills Acquired: System level modelling and verification

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1			3	3		2
CO 2			3	3	3	2
CO 3			3	3	3	2
CO 4			3	3	3	2

Syllabus

Unit 1:

Introduction to Electronic System Level Design–Design Space Exploration - Hybrid Design – ESLD Flows and Methodologies – Architecture Exploration–Hardware-software Partitioning.

Unit 2:

Models for ESL Design– Open-Source Language–SpecC (basic idea), System C –Transaction Level Modelling- Building Platform Models- High Level Synthesis-– Power Evaluation — Virtual Platform and Virtual Prototyping.

Unit 3:

Functional Models- High Level verification- Formal solution- Debugging Platform Models Case study: Bluespec and Accellera initiatives on test and stimulus standards- Property Specification Language.

Reference(s)

1. Sandro Rigo, Rodolfo Azevedo and Luizsantos, *Electronic System Level Design – An Open Source Approach*, Springer, 2011.
2. Bailey, Brian, and Grant Martin. "*ESL Models and their Application*." Springer, Boston, MA, Springer, USA, DOI 10 (2010): 978-1.

3. David Black, Jack Donovan, Bill Bunton and Anna Keist, "*System C from the ground up", Second Edition*, Springer, 2010.

25VL736 Low Power VLSI Circuit Design 3-0-0-3

Course Objectives

- To provide a comprehensive idea about different sources of power dissipation in VLSI circuits.
- To introduce the different power estimation and optimization methods.
- To apply low power techniques at all levels of the design cycle.

Course Outcomes: At the end of the course, the student should be able to
CO1 Ability to understand the concepts of low power VLSI circuits.
CO2 Ability to apply various architectures for low power implementations.
CO3 Ability to analyse the various power optimization techniques.
CO4 Ability to evaluate the power dissipation in VLSI circuits.

Skills Acquired:
Provide an understanding to analyse the different low power architectures

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	2	-	2	2
CO 2	-	-	2	2	2	2
CO 3	-	-	3	2	2	2
CO 4	-	-	2	2	2	2

Syllabus

Unit 1:

Importance of Low Power Consumption - Design for Low Power - Deep Submicron and Nanometer MOS Transistors and Models - Sources of Static and Dynamic Power Consumption in MOS Devices - New Device Technologies for Reducing Leakage Current - Basics of Power and Energy.

Unit 2:

Power Optimization During Design Cycle - Architecture - Algorithm and System Levels Power Optimization of Interconnects and Clocks - Dynamic Voltage Scaling - Clock Distribution - RTL Power Estimation and Optimization - Model Granularity - Model Parameters - Model Semantics - Model Storage and Model Construction.

Unit 3:

Power Optimization in Memories - Power in Cell Arrays - Power for Read and Write Accesses - Low Power Memory Technologies - Standby Power Optimization of Circuits and Systems -

Power Optimization of Circuits and Systems During Operation - Low Power Design Methodologies and Flows - Power Characterization and Modeling - Low Power Clock - Data and Power Gating.

Reference(s)

1. Jan M. Rabaey, *Low Power Design Essentials*, Springer, 2009.
2. Christian Piguet, *Low-Power CMOS Circuits: Technology, Logic Design and CAD Tools,* CRC Press, Taylor and Francis, 2006.
3. Rakesh Chadha and J. Bhaskar, *An ASIC Low Power Primer, Analysis, Techniques and Specification,* Springer, 2013.
4. Michael Keating, David Flynn, Robert Aitken, Alan Gibbons and Kaijian Shi, *Low power Methodology Manual for System on Chip*, Springer, 2007.
5. Kaushik Roy and S.C. Prasad, *Low power CMOS VLSI circuit design*, Wiley, 2000.

25VL737 System-on-Chip & FPGA Testing 3-0-0-3

Course Objectives

- To introduce the modules of System-on-chip.
- To impart knowledge on the FPGA Architecture.
- To comprehend the testing process on architectures.

Course Outcomes: At the end of the course, the student should be able to

CO1: Ability to comprehend the concept of System-on-chip.
CO2: Ability to apply testing process on System-on-chip testing.
CO3: Ability to analyze the challenges in FPGA architectures and FPGA Testing.
CO4: Ability to design for testability and built-in test architectures.

Skills Acquired: Knowledge on System on Chip (SOC) Testing and FPGA Testing.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1			2		2	
CO 2			3	3	3	
CO 3			3	2	3	
CO 4			3	3	3	

Syllabus

Unit 1:
Need of SOC testing – Basics of SOC- SOC Design Example – Scan Architectures – Logic Built-In-Self-Test – Aspects of SOC Testing – Modular – Wrapper –TAM-Scheduling – Modular – Wafer Sort and pre-burn-in test

Unit 2:
Introduction to FPGA Testing – FPGA architectures, FPGA Testing – Methods of Testing – Built-In-Self-Test of Resources – Testing - Embedded process, FPGA testing challenges.

Unit 3:
Modeling of Electrical parameter – Power issues – Low power scan testing – Low power BIST – Low power RAM Test – Built In Logic block observer – Design – SOC testing – PNX8550 – Case Studies

Reference(s)

1. L-T Wang, C. E. Stroud, & N. A. Touba, Editors, *System-on-chip Test architectures Nanometer design for testability*, Morgan Kaufmann Publishers, imprint of Elsevier, 2008.
2. Parag K. Lala, *An Introduction to Logic Circuit Testing*, Morgan & Claypool Publishers, 2009.
3. Cheng-Wen Wu, Chih-Tsun Huang, *Essential Issues in SOC Design*, Youn- Long Steve Lin, Editors, Soc Testing and Design for Testability pp 265-310, 2006.

25VL738 **Hardware Security and Trust** **3-0-0-3**

(*Pre-requisite: Digital Circuits and Systems)*

Course Objectives

- To introduce security and trust issues associated with hardware systems.
- To provide a background for recommending countermeasures for security and trust vulnerabilities.
- To impart experience in the design and implementation of security and trust primitives on both ASIC and FPGA.
- To impart knowledge aimed towards devising security and trust design and evaluation processes.

Course Outcomes: At the end of the course, the student should be able to
CO1: To understand various threats in Hardware systems due to hardware Trojans.
CO2: To apply various techniques to detect Hardware Trojans and securing designs.
CO3: To analyze various design for security methods.
CO4: To evaluate the requirements of reconfigurable hardware and security countermeasures.

Skills Acquired: Will acquire knowledge to design hardware with integrated security features, and ensure trustworthiness of VLSI circuits.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1			3	2	2	
CO 2			2	2	-	
CO 3			3	2	2	
CO 4			2	-	2	

Syllabus

Unit 1:

Introduction to hardware security and trust – Basics of VLSI Design and Test - Integrated Circuits (IC) Trojans – Taxonomy – Multi level attacks – Vulnerabilities in Combinational and Sequential Logic – Design for Hardware Trojans –Combinational Trojans – Synchronous and Asynchronous Counter-based Sequential Trojan – Hardware Trojan Insertion – Emerging applications and the new threats.

Unit 2:

Side-Channel Attacks include Power Spectrum Analysis – EM Analysis – Timing and Delay Analysis – Self-Referencing Methodology – Analysis of Process Variations – Fault Injection and Attacks - FPGA Security Attacks – Physical Attacks on FPGA and Countermeasures.

Unit 3:
Hardware security primitives – Physically Unclonable Functions (PUFs) – PUF Taxonomy – Delay Based PUFs – Memory-based PUF – Ring Oscillator PUF (RO-PUF) – Fault Attacks on PUFs – Privacy in PUF - True Random Number Generators (TRNG) – Protection of Intellectual Property (IP) – Watermarking Techniques for IP Protection – Quantum Resistance Cryptography - Validation of Security and Trust

Reference(s)

1. M. Tehranipoor and C. Wang, *Introduction to Hardware Security and Trust*, Springer, 2011.
2. Debdeep Mukhopadhyay, Rajat Subhra Chakraborty, *Hardware Security Design, Threats, and Safeguards*, Chapman & Hall, CRC Press, Taylor and Francis book, 2015.
3. Prabhat Mishra, Swarup Bhunia, Mark Tehranipoor, *Hardware IP Security and Trust*, Springer, 2017.
4. Edward Suh and S. Devadas, *Physical Unclonable Functions for Device Authentication and Secret Key Generation*, DAC-2007.
5. Badrignans, B., Danger, J.-L., Fischer, V., Gogniat, G., Torres, L. (Eds.), *Security Trends for FPGAs - From Secured to Secure Reconfigurable Systems*, Springer, 2011.

25VL741 VLSI Fabrication 3-0-0-3

Course Objectives

- Explain the motivation behind device scaling and its implications on power, performance, and process complexity and describe the processes for silicon wafer fabrication starting from sand, including crystal growth.

- Analyze each unit process in VLSI fabrication (such as crystal growth, oxidation, lithography, etching, ion implantation, and deposition), including physical principles, process parameters, and equipment used, and compare them.
- Interpret and model the impact of scaling on fabrication processes such as lithography resolution, doping profiles, deposition of thin films, and interconnect delay
- Design and propose process flows for fabricating MOSFET and FinFET devices.

Course Outcomes: At the end of the course, the student should be able to:

CO1: Understand the historical evolution and current trends in VLSI scaling, including the impact of Moore's Law and technology node transitions on circuit performance.

CO2: Understand the various unit processes, and models involved in the fabrication of semiconductor ICs such as Crystal Growth, Wafer Cleaning, Thermal Oxidation, Thin Film Deposition, Photolithography, Etching, Ion Implantation and Diffusion, and materials used.

CO3: Analyze the effect of process parameters on device fabrication and analyze the impact of continued scaling on each of the unit processes, and materials to be used.

CO4: Evaluate the materials, and technology used for Contacts, and Interconnects, and the impact of scaling on back-end processing and CMOS Process Flows

Skills Acquired: Provide an in-depth knowledge on how an IC is fabricated.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	3	2	-	-	-	-
CO 2	3	-	2	-	2	-
CO 3	3	3	2	2	2	-
CO 4	3	2	3	-	2	2

Syllabus

Unit 1:

Scaling Trends and Methodologies, Motivation for continued scaling of device dimensions, ITRS Road map, Si and GaAs Structure, Properties, Crystalline Directions, Sand to Silicon, Single Crystal Growth – CZ – Float Zone growth - Bridgman Growth, CMP & Polishing of Si Ingot, Gettering; Thermal Oxidation Process - Deal Groove Model - Linear and Parabolic Rate Coefficients - Oxide Characterization; Photolithography - Optical Lithography - Positive/ Negative Photoresists, Photo Masks, Types of Pattern Transfer, Diffraction Limits – Rayleigh Criterion, Light sources

Unit 2:

Extreme UV Lithography, Modulation Transfer Function, Spatial Coherence, Advanced Mask Techniques – Phase shift mask, Optical proximity correction, Antireflective coating; Photoresists – Components of Resist, DQN Photoresist, Resist Contrast and Critical Modulation Transfer Function, Resists for EUV lithography; Etching – Etch Metrics - Wet Chemical Etching - Plasma Assisted Etching - RIE – High Density Plasma – DRIE process - CMP; Ion Implantation – process and system – Mass Analyzer – Ion Stopping - Implantation Profile and control -

Deviations from Gaussian Profile – Skewness, Kurtosis, Ion Channeling - Implant Damage – Rapid Thermal Annealing.

Unit 3:

Diffusion – Predoposition Diffusion and Drive-in diffusion – Boundary Conditions and Solutions – Diffusion profile as a function of time and temperature – Diffusion Mechanism; Thin Film Deposition – Step Coverage and Aspect Ratio – PVD (Evaporation and Sputtering) process and tools, CVD techniques – LPCVD, PECVD, MOCVD, ALD – Film deposition rate; Epitaxial Growth Techniques – Vapor Phase Epitaxy and Molecular Beam Epitaxy - Structures and Defects in Epitaxial layers – Surface Preparation – Strained Silicon; Contacts and Metallization – RC delay – materials and process for Local and Global Interconnects – Diffusion Barrier – Intermetal Dielectrics - SOI Technology – MOSFET and FinFET process Flows – Sustainability in semiconductor manufacturing.

Reference(s)

1. Stephen Campbell, Stephen: *Fabrication Engineering at the Micro- and Nanoscale*, Oxford University Press, 4th Edition, 2013.
2. Peter Vanzant, Microchip Fabrication: *A Practical Guide to Semiconductor Processing,* Sixth Edition, McGraw Hill Professional, 2014.
3. Hong Xiao: *Introduction to Semiconductor Manufacturing Technology*, SPIE Publication, 2nd edition, 2012.
4. Gary. S. May, Costas J. Spanos: *Fundamentals of Semiconductor Manufacturing and Process Control*, First Edition, John Wiley, 2006
5. Robert Doering and Yoshio Nishi: *Handbook of Semiconductor Manufacturing Technology*, CRC Press, 2nd Edition, 2007
6. James D. Plummer, Michael D. Deal, Peter B. Griffin, *Silicon VLSI Technology: Fundamentals, Practice and Modeling,* Prentice Hall India Private Limited, 2000.

25VL742 Physical Design 3-0-0-3

Course Objectives

- To acquire knowledge of Physical design of simple logic gates using CMOS transistors.
- To provide knowledge involved in Partitioning, floorplanning, placement, clock tree synthesis, routing, and extraction of layout.
- To provide knowledge on the EDA tools used for Back end design of ICs.

Course Outcomes: At the end of the course, the student should be able to
CO1: Understand the back end flow of VLSI design cycle.
CO2: Apply techniques for ASIC design flow using standard cell libraries.
CO3: Apply the simple optimization techniques in the back end ASIC design flow.
CO4: Analyze and comprehend the physical design flow and related design, synthesis, test and timing issues.

Skills Acquired: Provide a practical approach for design of Application Specific Integrated Circuits, using Synopsys/Cadence EDA tool flow.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	3	-	-	-
CO 2	2	-	3	-	-	-
CO 3	2	-	3	3	-	-
CO 4	2	-	3	3	-	2

Syllabus

Unit 1:
Introduction to Physical IC Design–Objectives–VLSI Physical Design Cycle - CMOS circuit and layout design –Partitioning algorithms–Floor Planning algorithms– Specific Floor Planning Problems - Pin assignment.

Unit 2:
Placement: Constraints and algorithm - Timing Analysis: Clock Design - Clock Distribution Networks - Clock Tree Synthesis - Clock Power Analysis - Routing methodology: Grid Routing- Global Routing - Detail Routing - Channel Routing Problem.

Unit 3:
Analysis and Optimization Types–Best/Worst Analysis –Parasitic Extraction (RC Extraction)– Resistance extraction, Capacitance extraction, Inductance and impedance (RLC) extraction- Final Validation– Net List Output–GDS2 Output.

Reference(s)

1. "*Digital ASIC Design, A Tutorial on the Design Flow*", Digital ASIC Group, October 20, 2005, Lund University.
2. Majid Sarrafzadeh, C. K. Wong , "*An introduction to VLSI physical design*", McGraw Hill, 1996, ISBN 0070571945, 9780070571945, 334 pages
3. Khosrow Golshan, "*Physical design essentials: an ASIC design implementation perspective*", Springer, 2007, ISBN 0387366423, 9780387366425, 211 pages
4. Ban P. Wong, Anurag Mittal, Yu Cao, Greg Starr Contributor Ban P. Wong, Anurag Mittal, Yu Cao, "*Nano- CMOS circuit and physical design*", John Wiley and Sons, 2004.
5. Andrew B. Kahng, Jens Lienig, Igor L. Markov, *From Graph Partitioning to Timing Closure*, Jin Hu, Springer 2011.
6. K. Golshan, *Physical Design Essentials: An ASIC Design Implementation Perspective*, Springer, 2010.

25VL743 Design for Manufacturability 3-0-0-3

Course Objectives

- Understand process technology constraints affecting VLSI design.
- Learn layout-level techniques to improve yield and performance.
- Develop skills to optimize designs for manufacturability and variability.
- Understand the impact of scaling and FinFET-era challenges on manufacturability.

Course Outcomes: At the end of the course, the student should be able to:

CO1: Explain the impact of process variations and manufacturing constraints on VLSI design.
CO2: Apply DFM rules and techniques to optimize physical layout for improved yield and manufacturability.
CO3: Analyze and simulate the effects of parasitics, lithography limitations, and metal density on circuit reliability and performance.
CO4: Evaluate DFM strategies using EDA tools and incorporate variation-aware design principles in the physical design flow.

Skills Acquired: Provide an in-depth knowledge on Design for Manufacturability

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	3	2	1	2	1	-
CO 2	2	3	3	2	3	-
CO 3	3	3	2	3	3	-
CO 4	2	2	3	3	2	-

Syllabus

Unit 1**:**

Fundamentals of DFM and Manufacturing Constraints - Introduction to VLSI scaling and DFM importance - Process variations: inter/intra-die, random/systematic - Yield loss mechanisms and yield modeling - Lithography limitations, RET (OPC, PSM), DRC vs model-based checks

Unit 2:

DFM-Aware Layout and Cell Design - Layout techniques: redundancy, dummy fills, antenna rules - Stress-aware and CMP-aware layout - Standard cell design with DFM in mind - Routing strategies: jogs, spacing, via optimization - Density rules, IR drop, electromigration, signal integrity

Unit 3:

Variation-Aware Design and EDA Tool Integration - Statistical design and variability modeling - Corner analysis, Monte Carlo simulation - DFM-aware P&R and sign-off –
Tool flows: Calibre DFM, Synopsys IC Validator, Cadence PVS - FinFET-aware design, machine learning for DFM, DTCO

Reference(s)

1. Sandeep Kundu and Aswin Sreedhar, *Nanoscale CMOS VLSI Circuits – Design for Manufacturability*, McGraw-Hill, 2010.
2. Charles C Chiang and Jamil Kawa, *Design for Manufacturability and Yield for Nano-scale CMOS*, Springer 2007.

3. Ban Wong, Franz Zach, Victor Moroz, Anurag Mittal, Greg Starr, Andrew Kahng, *Nano-CMOS Design for Manufacturability*, John Wiley & Sons, 2009.
4. Artur Balasinski, *Semiconductors Integrated Circuit Design for Manufacturability*, CRC Press (Taylor and Francis), 2012.

25VL744 Data Structures and Algorithms for VLSI 3-0-0-3

Course Objectives:

1. To introduce the fundamental concepts of data structures and algorithms as they apply to VLSI design.
2. To introduce advanced data structures and algorithms to optimize various design and analysis tasks in VLSI.
3. To provide exposure to analysis and optimization VLSI circuit designs using algorithms that manage complexity and improve efficiency in layouts, routing, and placement.
4. To inculcate problem-solving skills using advanced data structures and algorithms to solve real-world VLSI design issues.

Course Outcomes: By the end of the course, students will be able to:

CO1: Design and implement algorithms for basic data structures such as trees, graphs, and lists tailored to VLSI problems.
CO2: Analyze and solve VLSI-related problems using algorithms
CO3: Apply computational geometry techniques in the design of VLSI systems
CO4: Apply optimization algorithms for performance and resource utilization in VLSI systems.

Skills Acquired: Algorithm Design and Analysis, VLSI Problem-Solving, Computational Geometry, Optimization Techniques.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	2			2		
CO 2	3		3	3		2
CO 3	3	2	3	3	2	3
CO 4	3	2	3	3	2	3

Syllabus:

Unit 1:

Introduction to VLSI and Algorithms - Basics of Data Structures - Linked lists, stacks, queues, trees, and graphs - Recursion and its applications in VLSI - Arrays and hash tables in VLSI applications. Graph Algorithms for VLSI - Shortest path algorithms (Dijkstra, Bellman-Ford) - Minimum spanning tree (Kruskal, Prim's) - Applications in routing and layout.

Unit 2:

Computational Geometry in VLSI - Geometric data structures and algorithms - Convex hulls, Voronoi diagrams, and polygon clipping - Applications in floor planning and placement. Divide and Conquer Algorithms in VLSI - Merging, quicksort, and closest pair problems - Partitioning algorithms for circuit design - Divide and conquer in circuit routing.

Unit 3:

Dynamic Programming and Greedy Algorithms - Overview of dynamic programming - Applications in sequence alignment, partitioning, and optimization - Greedy algorithms for wire-length minimization. VLSI Routing Algorithms - Maze routing and channel routing - Line search. Case studies in VLSI Applications.

Reference(s)

1. Sabih H Gerez, "*Algorithms for VLSI Design Automation*", Wiley, 1998
2. Naveed A Shervani, "*Algorithms for VLSI Physical Design Automation*", Springer, 2013
3. Thomas H. Cormen, Charles E. Leiserson, Ronald L. Rivest, and Clifford Stein, "*Introduction to Algorithms*", MIT Press, 2009
4. Mark de Berg, Otfried Cheong, Marc van Kreveld, and Mark Overmars, "*Computational Geometry: Algorithms and Applications*", Springer, 2010.

25VL745 Static Timing Analysis 3-0-0-3

Course Objectives

- To introduce timing analysis and apply it to constrain a design.
- To impart knowledge on cell delay calculation and parasitic extraction.
- To provide a practical approach for configuring static timing environment.
- To analyze a timing report and check for timing violations.

Course Outcomes: At the end of the course, the student should be able to
CO1: Understand the process of timing analysis in circuits and system design.
CO2: Apply wire load models to compute the cell delay and slack.
CO3: Analyze the circuit for design violations by configuring the timing environment.
CO4: Evaluate the system and perform timing verification.

Skills Acquired: Practical knowledge on timing analysis of designs using standard tools like Synopsys Prime Time.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	3	2	-	2
CO 2	-	-	3	3	2	3
CO 3	-	-	3	3	3	3
CO 4	-	-	3	3	3	3

Syllabus

Unit 1:
Introduction to STA – STA Concepts - Standard Cell Library - Pin Capacitance - Timing Modeling - Timing Models - Combinational and Sequential Cells - State Dependent Models - Advanced Timing Modeling - Power Dissipation Modeling - Other Attributes in Cell Library - Characterization and Operating Conditions - Interconnect Parasitics.

Unit 2:
Delay Calculation - Overview - Cell Delay using Effective Capacitance - Interconnect Delay - Slew Merging - Different Slew Thresholds - Different Voltage Domains - Path Delay and Slack Calculation - Crosstalk and Noise - Glitch Analysis - Delay Analysis - Computational Complexity - Noise Avoidance Techniques.

Unit 3:
Configuring the STA Environment - Timing Verification - Setup and Hold Timing Check - Multicycle - False - Half Cycle Paths - Removal and Recovery Timing Checks - Timing Across Clock Domains - Multiple Clocks - Interface Analysis -On-Chip Variations- Time Borrowing- Back annotation-Sign-off Methodology- Statistical Static Timing Analysis.

Practical : EDA tools analysis – Setup and hold time violation and design remedies – Critical Path Analysis-Basic Clock Tree Synthesis flow- Determining Maximum frequency of operation

Reference(s)

1. J. Bhasker, R.Chadha, *Static Timing Analysis for Nanometer Designs: A Practical*
2. *Approach*, First edition, Springer, 2009.
3. Charles J. Alpert Dinesh P. Mehta Sachin S. Sapatnekar, *Handbook of Algorithms for Physical Design Automation*, First edition, CRC Press, 2008.
4. Himanshu Bhatnagar, *Advanced ASIC Chip Synthesis Using Synopsys Design Compiler Physical Compiler and Prime Time*, Second Edition, Springer, 2002.
5. Sridhar Gangadharan, Sanjay Churiwala, *Constraining Designs for Synthesis and Timing Analysis: A practical Guide to Synopsys Design Constraints*, Springer, 2015.
6. R.Jayagovwri, Pushpendra S Yadav, *Static Timing Analysis for VLSI Circuits*, Second Edition, Medtech, Scientific International Publisher,2024.

25VL746 Machine Learning for VLSI 3-0-0-3

Course Objectives

- Understanding core Machine Learning concepts and algorithms
- Applying Machine Learning concepts to VLSI design challenges
- Developing practical skills using Machine Learning algorithms in VLSI design process

Course Outcomes: At the end of the course, the student should be able to

CO1: Identify the goals, applications, types and design issues of machine learning techniques.
CO2: Discover shell script programmatically using different features and debugging the code
CO3: Describe machine learning in VLSI EDA for automation.

Syllabus:

Unit 1:

Introduction: Aims and applications of machine learning, Linear and Logistic Regression, Instance based learning, Bayesian learning, Support Vector Machine, Kernel function.

Unit 2:

Learning Algorithms Scripting concepts, Shell responsibilities, OS, h/w, kernel, File system, passing arguments, Process, Networking, Version control processes.

Unit 3:

Taxonomy for Machine Learning in VLSI Design-Scope of machine learning in VLSI Physical Design. Machine Learning for Fabrication. Lithographic Process Models: Masks, and Physical Design, Yield Enhancements. Logic Synthesis and Physical Design, Verification and testing, Machine Learning-Based Aging Analysis

Skills Acquired: Use of Machine learning in VLSI Design and Automation

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	3	2	1	2	1	-
CO 2	2	3	3	2	3	-
CO 3	3	3	2	3	3	-
CO 4	2	2	3	3	2	-

Reference(s)

1. Ethem Alpaydın, *Introduction to Machine Learning* , MIT Press, 4th Edition, 2020.
2. Guyue Huang, Jingbo Hu, et al., *Machine Learning for Electronic Design Automation: A Survey. ACM Trans. Des. Autom. Electron*. Syst. 26, 5, Article 40 (September 2021)
3. *Shell Programming in Unix, Linux and OS X*: The Fourth Edition of Unix Shell Programming, Stephen G. Kochan, Patrick H. Wood, Addison-Wesley, 2016.
4. "*Machine Learning in VLSI Computer-Aided Design*", Ibrahim (Abe) M. Elfadel Duane S. Boning Xin Li, Springer International Publishing, 2019.

25VL747 MEMS Technology 3-0-0-3

Course Objectives

- To impart knowledge on microfabrication techniques for MEMS applications.
- To familiarise with the operation principles of selected MEMS Sensors and Actuators
- To introduce interdisciplinary understanding of engineering and materials science in MEMS development.

Course Outcomes: At the end of the course, the student should be able to
CO1: able to understand the world of microelectromechanical devices and systems
CO2: able to gain fundamental knowledge on material properties and fabrication technologies
CO3: able to comprehend working principles of sensing and actuation
CO4: able to design micro-devices using the MEMS fabrication process

Skills Acquired: Application of microfabrication and design for MEMS sensors and actuators.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-		2	2	2
CO 2	-	-		3	3	2
CO 3	-	-		2	3	2
CO 4	-	-		3	3	3

Syllabus

Unit 1:

Introduction to MEMS Technology, Historical perspective and evolution, Design considerations and constraints, Scaling laws and miniaturization challenges, Materials for MEMS applications and their properties– Silicon, glass, polymers and metals, Bulk and Surface Micro-machining techniques. Etching, Deposition (CVD/PECVD), Evaporative Sputtering, Electroplating, Electroless-plating.

Unit 2:

Photolithography, Advanced lithography techniques, Wet and Dry Etching Methods, Isotropic Etching and Anisotropic Etching, Wafer-Bonding, Packaging, High Aspect-Ratio Processes (LIGA) Techniques, Characterisation techniques – Electrical, mechanical characterization

Unit 3:

MEMS Pressure, Accelerometers and Flow sensors, Electrostatic sensing and actuation principles, thermal sensing and actuation principles, Piezoresistive/Piezoelectric sensing principles, Optical sensing and actuation, BioMEMS - Lab-on-a-chip systems, Wearable systems for health monitoring, bio-compatible materials.

Reference(s)

1. Tai-Ran Hsu, *MEMS and Microsystems – Design, Manufacture, and Nanoscale Engineering*, John Wiley & Sons, Inc., Hoboken, New Hersey, 2008
2. Marc J. Madou, *Fundamentals of Microfabrication – The Science of Miniaturization*, CRC Press, 2018.
3. Samira Hosseini, Michelle Alejandra Espinosa-Hernandez, Ricardo Garcia-Ramirez, Ana Sofia Cerda-Kipper, Sofia Reveles-Huizar, Luis Acosta-Soto, *BioMEMS – Biosensing Applications*, Springer, 2021

4. Julian W. Gardner and Vijay K. Varadan, "*Microsensors, MEMS and Smart Devices"* ,John Wiley &Sons, Inc. New York, NY, USA 2001.

25VL748 VLSI Packaging Technologies and Design 3-0-0-3

Course Objectives

- To introduce basic concepts and types in Microchip Packaging
- To understand how packaging needs vary for various applications.
- To understand the thermal, mechanical, electrical, and chemical degradation mechanisms that affect the reliability of packaged devices.

Course Outcomes: At the end of the course, the student should be able to
CO1: Understand various IC packaging techniques.
CO2: Understand constraints in each technique and modifications needed in extending these to various applications.
CO3: Understand various reliability test strategies used in packaging.
CO4: Understand the reliability issues in packaging.

Skills Acquired: Provide an in-depth knowledge on how an IC package is done.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	2	-	-	-
CO 2	-	-	3	2	-	-
CO 3	-	-	2	2	-	-
CO 4	-	-	3	2	-	-

Syllabus

Unit 1:

General Packaging Principles –Wire Bonding – Flip Chip Technologies –Types of Packaging – Ball Grid Array – Quad Lead – Surface Mount Technology –Monolithic 3D ICs.

Unit 2:

Component Packaging (Including Integrated Circuits, Opto, MEMS, RF and Solar Devices) – Substrates used in Packaging –Electrical and Thermal Considerations.

Unit 3:

Reliability Test Strategies –Reliability Modelling –Reliability Testing, Degradation and Failure Mechanisms – MTTF, FIT, Thermal – Chemical – Electrical and Mechanical – Characterization Techniques.

Reference(s)

1. Vasilis F. Pavlidis, IoannisSavidis and Eby G. Friedman, *Three dimensional Integrated Circuit Design* Second Edition., Morgan Kaufmann, 2017.
2. Milton Ohring and Lucian Kasprzak, *Reliability and Failure of Electronic Materials and Devices*, Second Edition, Academic Press, 2014.
3. Chuan Seng Tan, Kuan-Neng Chen and Steven J Koester, 3D *integration for VLSI Systems*, Pan Stanford Publishing, CRC Press, 2012.
4. Andrea Chen and Randy Hsiao-Yu Lo, *Semiconductor Packaging: Materials Interaction and Reliability*, CRC Press, 2012.
5. Richard K. Ulrich and William D. Brown, *Advanced Electronic Packaging*, John Wiley & Sons, Inc., 2006.

25VL751 VLSI Architectures for Multicore and Heterogeneous Computing 3-0-0-3

Course Objectives

- To introduce approaches to parallelism in modern processors.
- To impart background in communication and memory management schemes in
- multicore systems.
- To provide grounding in the fundamentals of heterogeneous computing systems.
- To introduce typical paradigms in heterogeneous systems.

Course Outcomes: At the end of the course, the student should be able to
CO1: Ability to understand approaches to parallelism in processors.
CO2: Ability to apply parallel approaches to analyze computing systems.
CO3: Ability to analyze the impact of communication and memory architectures on performance.
CO4: Ability to evaluate the design requirements of applications to be implemented in computing platforms

Skills Acquired: provide in depth knowledge on heterogeneous architectures
CO-PO Mapping:

CO/PO	PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	2
CO2	2	-	3	3	-	2
CO3	2	-	3	3	-	2
CO4	2	-	3	3	-	2

Syllabus

Unit 1:

Review of Types of Parallelism - Instruction Level Parallelism - Thread Level Parallelism - Limits of ILP - Parallel Processing Architectures - Superscalar - VLIW - Scheduling - Techniques - Static and Dynamic Schemes - SIMD Architectures - GPU.

Unit 2:

Inter-Processor Communication Schemes - Bus-Based - Shared Memory – Distributed Memory and Network on Chips - Performance Analysis - Data Parallelism - GPU and GPGPU Applications - Overview of HPC Platforms

Unit 3:

Introduction to Markovian/Stochastic Models for Heterogeneous Computing – Operating System - Role of Multi-Cores - Case Study for Heterogeneous Architectures - Case Studies of Data-Intensive Application Platforms - FPGA based Platforms.

Reference(s)

1. Hennesey and Patterson, *Computer Architecture: A Quantitative Approach*, Sixth Edition , Morgan Kaufmann, 2018.
2. K. Uchiyama, F. Arakawa, H. Kasahara, T. Nojiri, H. Noda, Y. Tawara, A. Idehara, K. Iwata and H. Shikano, *Heterogeneous Multi-core Processor Technologies for Embedded Systems*, Springer, 2012.J.
3. Dongarra and A.L. Lastovetsky, *High Performance Heterogeneous Computing*, Wiley Series, 2009.
4. Abderazek Ben Abdallah, *Advanced Multicore Systems-On-Chip: Architecture, On-Chip Network*, Design, Springer 2017.
5. Journals, White papers and Technical Reports in the area of High-Performance Parallel computing.

25VL752 Reconfigurable Computing 3-0-0-3

Course Objectives

- Understanding the principles of reconfigurable architectures
- Designing and implementing systems on reconfigurable hardware like FPGAs.
- Exploring applications that benefit from dynamic hardware reconfiguration

Course Outcomes: At the end of the course, the student should be able to

CO1: Understand fundamental concepts and the evolution of reconfigurable architectures.
CO2: Analyse various FPGA architectures and tools.
CO3: Apply high-level synthesis and hardware/software co-design methodologies.
CO4: Design reconfigurable systems for real-world applications and evaluate trade-offs.

Skills Acquired: in-depth knowledge in various reconfigurable architectures
CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO1	-	-	2	-	-	-
CO2	-	-	2	-	-	-
CO3	-	-	3	3	2	-
CO4	-	-	3	3	2	-

Syllabus:

Unit 1:

Introduction to Reconfigurable Computing - Mask-programmed to field-programmable; Suitability for parallel processing; Domain-specific acceleration- General Purpose Processors (GPP), ASICs, FPGAs; Fixed vs adaptive hardware; Comparison with GPUs and DSPs- Fine-grain (bit-level, LUTs) vs coarse-grain (word-level, ALUs); Granularity impact on power, speed, area; Reconfigurable datapaths.

Unit 2:

Basic FPGA Architecture- Configuration Technologies- Overview of Xilinx, Intel (Altera), Lattice, Microsemi; FPGA families: Spartan, Artix, Kintex, Virtex, Zynq, Cyclone, Stratix; Real-world board-level examples- Configuration Methods- JTAG, Slave/Passive Serial, SelectMAP, SPI; Configuration bitstream structure; Concept of Partial Reconfiguration (PR): spatial, temporal- Traditional FPGA Design Flow - Placement and Routing - Simulation and Verification- - Emerging Trends in reconfigurable architectures

Unit 3:

High-Level Synthesis (HLS)- Loop pipelining and latency constraints - Hardware/Software Co-design- Task partitioning basics; Memory-mapped I/O communication; Integration with soft/hard processors- Introduction to AXI interface; Use of standard IPs (FIFO, memory controllers); IP packaging; Xilinx IP Integrator/Qsys overview - Soft-core Processors on FPGA - SoC and MPSoC FPGA Platforms - Partial and Dynamic Reconfiguration - Reconfigurable Computing Applications and case studies

References(s)

1. Scott Hauck and André DeHon, *Reconfigurable Computing: The Theory and Practice of FPGA-Based Computation*, Morgan Kaufmann, 2007.
2. Frank Vahid, *Digital Design with RTL Design, VHDL, and Verilog*, Wiley, 2010.
3. Clive Maxfield, *The Design Warrior's Guide to FPGAs*, Newnes, 2004.
4. Wayne Wolf, *FPGA-Based System Design*, Prentice Hall, 2004.
5. Hubertus Franke et al., *High-Performance Reconfigurable Computing*, Springer, 2021.
6. Vendor docs: Xilinx Vivado/Vitis, Intel Quartus Prime, ARM Cortex integration guides.

25VL753 Network on Chip 3-0-0-3

Course Objectives

- To provide basic concepts of NoC design by introducing the topologies, router design and MPSoC styles.
- To introduce sample routing architectures with evaluation and routing algorithm on a NoC.
- To provide knowledge of the functions of reconfigurable NoC.
- To introduce 3D NoCs and its future trends.

Course Outcomes: At the end of the course, the student should be able to

CO1: Ability to understand the need for NoC, architectures, reconfiguration NoCs.

CO2: Ability to understand routing algorithms and flow control mechanisms.

CO3: Ability to analyze and design aspects of NoC architectures and reconfiguration techniques.

CO4: Ability to analyze and design aspects of NoC routing algorithms and flow control mechanisms.

CO-PO Mapping

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO1	-	-	2	-	-	-
CO2	-	-	2	-	-	-
CO3	-	-	3	3	2	-
CO4	-	-	3	3	2	-

Skills Acquired: Design aspects of NoC topologies, routing algorithms and reconfigurable NoCs.

Syllabus

Unit 1:

Introduction - On-Chip Vs. Off-Chip Networks - On-Chip Network Building Blocks. Interface with System Architecture - Shared Memory Networks in Chip Multiprocessors - Synthesized Nocs in MPSoCs. Topology - Direct Topologies - Indirect Topologies - Irregular Topologies. Routing Algorithms - Types - Oblivious Routing - Adaptive Routing - Source Routing - Node Table-Based Routing - Routing on Irregular Topologies.

Unit 2:

Flow Control - Message-based Flow Control - Packet-based Flow Control - Flit-based Flow Control - Flow Control Implementation in MPSoCs - Router Microarchitecture - Pipeline - Buffer Organization - Allocators and Arbiters - Architecture Design of Network-On-Chip - Wormhole Router Architecture Design - Adaptive Router Architecture Design.

Unit 3:

Evaluation of Network-On-Chip Architectures - Traffic Modeling - Localized Traffic - Reconfigurable Network-On-Chip Design - Local Reconfiguration Approach - Topology Reconfiguration - Link Reconfiguration - Three-Dimensional Integration of Network-on-Chip - Opportunities and Challenges of 3D Integration - Design and Evaluation of 3D NoC Architecture - Future Trends - Photonic NoC - Wireless NoC.

Reference(s)

1. Santanu Kundu, Santanu Chattopadhyay, *Network-on-Chip: The Next Generation of System-on-Chip Integration*, CRC Press, 2018.

2. N. Enright Jerger and L-S. Peh, *On-Chip Networks, Synthesis Lectures on Computer Architecture*, Morgan & Claypool, 2009.
3. Konstantinos Tatas, Kostas Siozios, Dimitrios Soudris, Axel Jantsch, *Designing 2D and 3D Network on Chip Architecture*, Springer, 2013.
4. A Jantsch and H. Tenhunen, *Networks on Chip*, Kluwer Academic Publishers, 2003.

25VL754 Hardware Software Co-Design 3-0-0-3

Course Objectives

- To introduce the design of mixed hardware-software systems.
- To explore fragmentation of hardware and software components from software modules.
- To learn transformations on hardware and software co-design architectures for real time hardware systems.

Course Outcomes: At the end of the course, the student should be able to
CO1: Ability to understand the need for hardware software co-design in the design flow process.
CO2: Ability to analyze hardware-software co-design problems for systems with moderate Complexity.
CO3: Ability to apply hardware-software co-design methods and techniques to practical problems.
CO4: Ability to apply different levels of abstractions and provide models for verification of the architecture and functionality for embedded co-design solutions.

Skills Acquired: Ability to apply co-design concepts in design flow for high-level specifications

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1			3	3		
CO 2			3	3		
CO 3			3	3	3	
CO 4			3	3	3	

Syllabus

Unit 1:

Introduction to Hardware/Software Co-design – Factors for Co-design – Design Space - Generic Co-Design Methodology – Co-design Architectures – Data Flow Modeling – Implementation

Unit 2:

Hardware/Software Co-Synthesis Algorithm – Partitioning – System Level Specification – Design and Languages – Hardware/Software Co-design using LYCOS system

Unit 3:

Co-design for Multi-Processor Architectures – Applications - FPGA Platforms of CORDIC Coprocessor – Crypto Processor – Case Studies

Reference(s)

1. Patrick R. Schaumont, *A Practical Introduction to Hardware/Software Co-design*, Second Edition, Springer, 2013.
2. Jorgen Staunstrup and Wayne Wolf, *Hardware/Software Co-design: Principle and Practice*, Kluwer Academic Publishers, 1997.
3. Giovanni De Micheli, *Readings in Hardware Software Co-design*, Morgan Kaufmann, Academic Press, 2002.
4. Sao-Jie Chen, Kuang-Huei Lin, Pao-Ann Hsiung and Yu-Hen Hu, *Hardware Software Co-Design of a Multimedia SOC Platform*, Springer, 2010.
5. *Vivado Design Suite User Guide: Embedded Processor Hardware Design* UG898 (v2017.3) October 27, 2017.
6. ACM Transactions on Design Automation of Embedded Systems.

25VL755 Embedded Computing and Programming 3-0-0-3

Course Objectives

- To introduce design concepts of embedded systems.
- To provide insights on embedded C programming for configuring microcontroller and peripherals
- To enable development of embedded system models.

Course Outcomes: At the end of the course, the student should be able to
CO1: Able to identify the features of STM32F microcontroller.
CO2: Able to apply embedded C programming skills for configuring STM32F peripherals.
CO3: Able to analyze external peripheral interfacing with a microcontroller.
CO4: Able to design and develop embedded systems using STM32F microcontroller.
Skills acquired: Provide detailed insight on configuration and programming of various peripherals in STM32 Microcontroller.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1			3	3		
CO 2			3	3		
CO 3			3	3	3	
CO 4			3	3	3	

Syllabus

Unit.1:

STM32F Processor: Introduction to Embedded Systems - Introduction to ARM - Advanced

RISC Features - Core Data path - Register Organization and Special Function Registers – STM32F System Architecture – Memory Organization – Clock Configuration and PLL - Low Power Modes - Power Control Registers - Backup Registers - Programming STM32F.

Unit.2:

STM32F Peripherals: Introduction to Embedded C Programming - GPIO: Modes, Speed, Pull Configurations, External Interrupts – Timers: Configuration, Counter Modes, Interrupts – PWM Generation using Timers – UART Communication: Polling and Interrupt-based – ADC and DAC Configuration – Triggering and Data Acquisition – SPI and I2C Communication Protocols – Nested Vectored Interrupt Controller (NVIC): Priorities and Interrupt Handling – HAL and LL Drivers – Code Generation using STM32CubeMX.

Unit.3:

External Peripheral Interfacing
LCD Interfacing: 16x2 and Graphical – Keypad Matrix: Scanning and Debouncing – Motor Control: DC, Stepper, Servo using PWM – EEPROM Interfacing via I2C/SPI – Sensor Interfacing: Analog and Digital Sensors (e.g., LM35, IR, LDR) – Seven Segment Display: Static and Multiplexed Modes – Embedded Application Design Cycle – Real-Time Considerations and ISR Optimization – Debugging using Serial Monitor, Logic Analyzer – Mini Project Development using STM32 and Peripheral Integration.

Reference(s)

1. Muhammad Ali Mazidi, STM32 *Arm Programming for Embedded Systems*, 2019.
2. Donald Norris, Programming with STM32: *Getting Started with the Nucleo Board and C/C++*, McGraw-Hill Education, 2018
3. *STM32F446xx advanced Arm*®-based 32-bit MCUs, Reference Manual, 2020

25VL756 Emerging Architectures for Machine Learning 3-0-0-3

Course Objectives

- To introduce new paradigms in computing.
- To familiarize various aspects and issues in implementation of machine learning systems.
- To impart background on application of FPGAs and unconventional computing platforms for machine learning.
- To provide exposure to using state of the art computing tools.

Course Outcomes: At the end of the course, the student should be able to

CO1: Ability to understand high performance machine learning architectures.
CO2: Ability to apply computing paradigms for machine intelligence problems.
CO3: Ability to suggest solutions and platforms for dataflow intensive problems.
CO4: Ability to evaluate the use of diverse technologies to design efficient applications.

CO-PO Mapping:

CO/PO	PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	2
CO2	2	-	3	3	-	2
CO3	2	-	3	3	-	2
CO4	2	-	3	3	-	2

Skills Acquired: Ability to develop architectures for Machine Learning.

Syllabus

Unit 1

Overview of Machine Learning and Deep Learning Models – Algorithm to hardware translation – Bitwidth – Fixed Point and Floating Point representations – Precision Effects

Unit 2
Least Mean Square Algorithm – Case Studies – Neural Network Implementations – Trade-offs

Unit 3
Advanced algorithms – Deep Learning implementations – Neuromorphic Architectures – Sparsity - Irregular Computations – Introduction to neuromorphic Architectures.

Reference(s)

1. Shiho Kim and Ganesh Chandra Deka, *Advances in Computers, Volume 122: Hardware Accelerator Systems for Artificial Intelligence and Machine Learning*, ScienceDirect, 2021
2. Andres Rodriguez, *Deep Learning Systems: Algorithms, Compilers, and Processors for Large-Scale Production.* Synthesis Lectures on Computer Architecture. Morgan & Claypool Publishers. Oct. 2020.
3. V. Sze, *Designing Hardware for Machine Learning*, in IEEE Solid-State Circuits Magazine, vol. 9, no. 4, pp. 46-54, Fall 2017 (paper)
4. Lei Deng, Guoqi Li, Song Han, Luping Shi, and Yuan Xie, *Model compression and hardware acceleration for neural networks: A comprehensive survey.* Proceedings of the IEEE 108, no. 4 (2020): 485-532. (paper)
5. Shail Dave, Riyadh Baghdadi, Tony Nowatzki, Sasikanth Avancha, Aviral Shrivastava, and Baoxin Li., *Hardware acceleration of sparse and irregular tensor computations of ML models: A survey and insights.* Proceedings of the IEEE 109, no. 10 (2021): 1706-1752. (paper)

25VL757 Cryptography 3-0-0-3

Course Objectives

- To provide basic knowledge and skills in the fundamental theories and practices of data security.
- To provide an overview of the field of security and emphasizing the need to protect information being transmitted electronically.
- To provide an understanding of the different cryptographic algorithms.
- To realize the hardware architectures of cryptographic algorithms

Course Outcomes: At the end of the course, the student should be able to

CO1: Understand the mathematical fundamental concepts needed for cryptographic algorithm implementations.

CO2: Apply concepts of security to computing systems

CO3: Analyze cryptosystems architecture, digital signature algorithms and secure data sharing techniques
CO4: Evaluate the implementation of cryptographic algorithms in FPGA.

Skills Acquired: Ability to use cryptographic algorithms for data security.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	3	3	-	2
CO 2	2	-	3	3	2	2
CO 3	2	-	3	3	2	2
CO4	3	-	3	3	3	3

Syllabus

Unit 1:
Introduction to Probability Theory– Information Theory – Complexity Theory and Number Theory – Private-Key – Cryptosystems – Classical Ciphers – DES Family – Product Ciphers – Lucifer Algorithm – Modern Private Key Cryptographic Algorithms – Differential Cryptanalysis – Linear Cryptanalysis – S-box Theory – Propagation and Nonlinearity – Construction of Balanced Functions.

Unit 2:
Public-Key Cryptosystems – RSA Cryptosystem – Merkle-Hellman Cryptosystem – McEliece Cryptosystem – ElGamal Cryptosystem – Elliptic Curve Cryptosystems – Probabilistic Encryption – Pseudo-Randomness – Polynomial Indistinguishability – Pseudorandom Bit Generators – Pseudorandom Function Generators – Super Pseudorandom Permutation Generators – Hashing – Theoretic Constructions – Hashing based on Cryptosystems – MD Family – SHA Family – Keyed Hashing.

Unit 3:

Digital Signature – Generic Signature Schemes –RSA Signatures – Elgamal Signatures – Blind Signatures – Undeniable Signatures – Fail-Stop Signatures – Time Stamping – Secret Sharing – Threshold Secret Sharing (T, T) –Threshold Schemes – Shamir Scheme – Blakley Scheme – Modular Scheme – General Secret Sharing – Stream Ciphers – Linear Complexity – Non Linear Feedback Shift Registers-VLSI Implementation of some of the Cryptographic algorithms.

Reference(s)

1. Josef Pieprzyk, Thomas Hardjono and Jennifer Seberry, *Fundamentals of Computer Security*, Springer, 2003.
2. Alfred J. Menezes, Paul C. Van Oorschot and Scott A. Vanstone, *Handbook of Applied Cryptography*, CRC Press, 1996.
3. Abhijith Das and VeniMadhavanC. E., *Public-key Cryptography, Theory and Practice*, Pearson Education, 2009.
4. Jonathan Katz and Yehuda Lindell, *Introduction to Modern Cryptography*, Third Edition, CRC Press, 2020.

5. Christof Paar, Jan Pelzl, *Understanding Cryptography: A Textbook for Students and Practitioners*, Springer, 2014.

25VL758 VLSI for IoT 3-0-0-3

Course Objectives

- To introduce IoT paradigm.
- To impart knowledge of IoT building blocks and their interactions.
- To provide exposure to typical approaches towards IoT VLSI system implementation.

Course Outcomes: At the end of the course, the student should be able to
CO1: Ability to understand the working of the Internet of Things.
CO2: Ability to develop IoT abstractions for real life problems.
CO3: Ability to identify building blocks for realizing IoT systems.

Skills Acquired: Design IoT solutions for applications by choosing appropriate VLSI platforms and design flows.

CO-PO Mapping:

CO/PO	PO1	PO2	PO3	PSO1	PSO2	PSO3
CO1	2	-	3	3	-	2
CO2	2	-	3	3	-	2
CO3	2	-	3	3	-	2
CO4	2	-	3	3	-	2

Syllabus

Unit 1:

Introduction to IoT - Features - IoT Stack - Technologies and IoT Challenges - Sensors and Hardware for IoT - Protocols.

Unit 2:

Model based Approaches - Hardware/Software Partitioning - Computing Paradigms/Platforms - IoT/Cloud Integration – Power Optimization

Unit 3:

Security aspects of IoT - Integrity - Confidentiality - Authenticity - Case Study of Design of a Typical IoT System

Reference(s)

1. Pethuru Raj and Anupama C. Raman, *The Internet of Things: Enabling Technologies, Platforms, and Use Cases*, CRC Press, 2017.
2. Adrian McEwen, *Designing the Internet of Things*, Wiley,2013.

3. Milan Milenkovic, *Internet of Things: Concepts and System Design*, Springer, 2020.
4. Cem Unsalan and Bora Tar, *Digital System Design with FPGA: Implementation Using Verilog and VHDL*, McGraw Hill,2017. Journals and White papers.

25VL759 VLSI Signal Processing 3-0-0-3

Course Objectives

- To introduce the concepts of DSP architecture design.
- To provide an understanding of the techniques needed for the implementation of DSP architectures.
- To emphasize the realization of DSP architectures with high throughput, less area and less power.
- To provide an understanding of the concepts of high performance VLSI system design.

Course Outcomes: At the end of the course, the student should be able to

CO1: Understand the various VLSI architectures for digital signal processing Algorithms.
CO2: Apply and analyze techniques of high level architectural transformation for designing DSP algorithms.
CO3: Apply and analyze the algorithmic transformation techniques for designing DSP algorithms.
CO4: Evaluate architectures for adders, multipliers and digital filters.

Skills Acquired: Provides skill needed for the usage of design methodologies for the realization of VLSI architectures for signal processing algorithms.

CO-PO Mapping:

CO/PO	PO 1	PO 2	PO 3	PSO1	PSO2	PSO3
CO 1	-	-	2	3	-	2
CO 2	2	-	2	3	2	2
CO 3	2	-	2	3	2	2
CO 4	2	-	3	3	2	3

Syllabus

Unit 1:

Introduction to Digital Signal Processing Systems - Iteration Bound - Pipelining and Parallel Processing – Retiming - Unfolding - Folding - Systolic Architecture Design.

Unit 2:

Fast Convolution - Algorithmic strength reduction - Pipelined and Parallel Recursive and Adaptive Filters - Scaling and Round off Noise - Digital Lattice Filter Structures.

Unit 3:

Bit-Level Arithmetic Architectures – Redundant Arithmetic –Numeric Strength Reduction – Low-Power Design – Case studies of algorithm to architecture mapping -performance – complexity trade-offs.

Reference(s)

1. Keshab K. Parhi, *VLSI Digital Signal Processing Systems, Design and Implementation*, John Wiley, 1999.
2. U. Meyer – Baese, *Digital Signal Processing with Field Programmable Arrays*, Springer, Fourth Edition, 2014.
3. S.Y.Kuang, H.J. White house, T. Kailath, *VLSI and Modern Signal Processing*, Prentice Hall, 1995.
4. Peter Pirsch, *Architectures for Digital Signal Processing*, Wiley, 2009.

25AVP501 MASTERY OVER MIND 1-0-2-2

PG SYLLABUS

COURSE OBECTIVES

Master Over the Mind (MAOM) is an Amrita initiative to implement schemes and organize university-wide programs to enhance health and wellbeing of all faculty, staff, and students (UN SDG -3). This program as part of our efforts for sustainable stress reduction introduces immediate and long-term benefits and equips every attendee to manage stressful emotions and anxiety facilitating inner peace and harmony. With a meditation technique offered by Amrita Chancellor and world-renowned humanitarian and spiritual leader, Sri Mata Amritanandamayi Devi (Amma), this course has been planned to be offered to all students of all campuses of AMRITA, starting off with all first years, wherein one hour per week is completely dedicated for guided practical meditation session and one hour on the theory aspects of MAOM. The theory section comprises lecture hours within a structured syllabus and will include invited guest lecture series from eminent personalities from diverse fields of excellence. This course will enhance the understanding of experiential learning based on university's mission: "Education for Life along with Education for Living" and is aimed to allow learners to realize and rediscover the infinite potential of one's true Being and the fulfilment of life's goals.

COURSE OUTCOME

After successful completion of the course, students will be able to:	
S.No.	**Course Outcomes**
1.	Understand the scientific benefits of meditation. (CO1)
2.	Explain the science behind meditation and its effects on physical and mental well-being (CO2).
3.	Understand the meditation techniques to cultivate emotional intelligence and improve relationships (CO3).
4.	Learn and practice MAOM meditation in daily life (CO4).
5.	To apply the effect of meditation to compassion-driven action (CO5)

Syllabus:

Scientific benefits of Meditation (CO1)

Scientific benefits of meditation, exploring its effects on physical and mental wellbeing.

Learn about the different types of meditation practices, the essential elements of meditation, and the empirical evidence supporting its benefits.

Video resource-Swami Atmanandamrita Puri

Science Behind Meditation (CO2)

A: A preliminary understanding of the Science of meditation. What can modern science tell us about this

tradition-based method?
B: How meditation helps humanity according to what we know from scientific research
Reading 1: Does Meditation Aid Brain and Mental Health (Dr Shyam Diwakar)
Reading 2: 'Science and Spirituality.' Chapter 85 in Amritam Gamaya (2022). Mata Amritanandamayi Mission Trust.

Role of Meditation in Emotional intelligence (CO3)

Learn how meditation practices can enhance self-awareness, self-regulation, motivation, empathy, and social skills, leading to improved relationships and decision-making. Improve communication, emotional intelligence, and interpersonal skills. Logical and analytical reasoning

Practicing MA OM Meditation in Daily Life (CO4)

Guided Meditation Sessions following scripts provided (Level One to Level Five)
Reading 1: MA OM and White Flower Meditation: A Brief Note (Swami Atmananda Puri)
Reading 2: 'Live in the Present Moment.' Chapter 71 in Amritam Gamaya (2022). Mata Amritanandamayi Mission Trust.

Meditation and Compassion-driven Action (CO5)

Understand how meditation can help to motivate compassion-driven action.
Reading 1: Schindler, S., & Friese, M. (2022). The relation of mindfulness and prosocial behavior:What do we (not) know? Current Opinion in Psychology, 44, 151-156.
Reading 2: 'Sympathy and Compassion.' Chapter 100 in Amritam Gamaya (2022). Mata Amritanandamyi Mission Trust.

Textbooks / References:

1. Mata Amritanandamayi Devi, "Cultivating Strength and vitality," published by Mata Amritanandamayi Math, Dec 2019
2. Swami Amritaswarupananda Puri," The Color of Rainbow "published by MAM, Amritapuri. 3. Craig Groeschel, "Winning the War in Your Mind: Change Your Thinking, Change Your Life" Zondervan Publishers, February 2019
4. R Nagarathna et al, "New Perspectives in Stress Management "Swami Vivekananda Yoga Prakashana publications, Jan 1986
5. Swami Amritaswarupananda Puri "Awaken Children Vol 1, 5 and 7 - Dialogues with Amma on Meditation", August 2019
6. Swami Amritaswarupananda Puri "From Amma's Heart - Amma's answer to questions raised during world tours" March 2018
7. Secret of Inner Peace- Swami Ramakrishnananda Puri, Amrita Books, Jan 2018.
8. Mata Amritanandamayi Devi "Compassion: The only way to Peace:Paris Speech", MA Center, April 2016.
9. Mata Amritanandamayi Devi "Understanding and collaboration between Religions", MA Center, April 2016.
10. Mata Amritanandamayi Devi "Awakening of Universal Motherhood: Geneva Speech" M A center, April 2016.

GLIMPSES OF INDIAN CULTURE

P/F

22ADM501: GLIMPSES OF INDIAN CULTURE

A. Prerequisite: nil

B. Nature of Course: Theory

C. Course Objectives:

- The course "Glimpses of Indian Culture" aims to provide students with a comprehensive understanding of various aspects of Indian culture, with a focus on its spiritual, philosophical, and religious dimensions.
- Through an exploration of the chapters from the provided book, students will gain insights into the foundational principles, practices, and symbols that shape the diverse cultural landscape of India
- Aligned with the Indian Knowledge Systems (IKS) framework outlined in the National Education Policy, this course serves as an introduction to the vast reservoir of wisdom and knowledge rooted in Indian heritage.
- By engaging with the chapters in the book, students will develop a holistic appreciation for the rich tapestry of Indian culture, spanning from its philosophical underpinnings to its artistic expressions, rituals, and societal values.
- This course aims to cultivate cultural sensitivity, critical thinking, and a deeper understanding of the diverse spiritual and cultural traditions that have shaped India's identity over millennia.

D. Course Outcomes: After successful completion of the course, Students will be able to:

CO	Course Outcomes	Knowledge level [Bloom's Taxonomy]
CO01	**Recall key concepts and terms associated with Sanatana Dharma, scriptures, and core cultural elements of India.** Statement: Demonstrate the ability to remember essential terms, concepts, and principles discussed in the chapters on Sanatana Dharma, scriptures, and cultural aspects.	Remembering
CO02	**Explain the concepts of Īśvara, Guru Tattva, Avatara Tattva, and the Theory of Karma as foundational elements of Indian cultural philosophy.** Statement: Understand the profound meanings of Īśvara, Guru, Avatara, and Karma, elucidating their importance in shaping Indian cultural thought.	Understanding
CO03	**Apply the knowledge of Purusharthas, Sanyasa, and Yajna to analyze real-life ethical and spiritual scenarios.** Statement: Utilize insights from Purusharthas, Sanyasa, and Yajna to navigate ethical dilemmas and make informed decisions**.**	Applying
CO04	**Analyze the symbolism in cultural practices, Nataraja iconography, and temple architecture.** Statement: Deconstruct the layers of symbolism in various cultural aspects, including Nataraja representation and temple architecture, unraveling their deep meanings.	Analyzing
CO05	**Evaluate the significance of temples as cradles of culture and explore alternative systems in India's cultural landscape.** Statement: Assess the role of temples in preserving cultural heritage and critically examine the diversity of cultural and spiritual systems in India.	Evaluating

CO06	**Develop projects or presentations that highlight the essence of Sanatana Dharma, sadhana, and the cultural significance of symbols.** Statement: Create expressive projects that capture the essence of Sanatana Dharma, convey the practices of sadhana, and portray the cultural meanings of symbols.	Creating

POs Programme Outcomes	**COs**
PO1: Engineering Knowledge **PO2: Problem Analysis** **PO3: Design/Development of Solutions** **PO4: Conduct Investigations of complex problems** **PO5: Modern tools usage** **PO6: Engineer and Society** **PO7: Environment and Sustainability** **PO8: Ethics** **PO9: Individual & Teamwork** **PO10: Communication** **PO11: Project management & Finance** **PO12: Lifelong learning** **B.Tech. EEE Programme Specific Outcome (PSO)** **PSO1:** Awareness of Future Technology: Develop solutions for future systems using smart technologies. **PSO2:** Research and Innovation: Identify engineering challenges, approach using cutting edge research tools and execute innovative solutions.	• CO 1: Recall key concepts and terms associated with Sanatana Dharma, scriptures, and core cultural elements of India. • CO 2: Explain the concepts of Īśvara, Guru Tattva, Avatara Tattva, and the Theory of Karma as foundational elements of Indian cultural philosophy • CO 3: Apply the knowledge of Purusharthas, Sanyasa, and Yajna to analyze real-life ethical and spiritual scenarios. • CO 4: Analyze the symbolism in cultural practices, Nataraja iconography, and temple architecture. • CO 5: Evaluate the significance of temples as cradles of culture and explore alternative systems in India's cultural landscape. • CO 6: Develop projects or presentations that highlight the essence of Sanatana Dharma, sadhana, and the cultural significance of symbols.

E. CO-PO Mapping: [affinity#: 3 – high; 2- moderate; 1- slightly]

COs	**Program Outcomes [POs]**												**Program Specific Outcomes [PSOs]***	
	PO1	**PO2**	**PO3**	**PO4**	**PO5**	**PO6**	**PO7**	**PO8**	**PO9**	**PO10**	**PO11**	**PO12**	**PSO1**	**PSO2**
CO01	-	-	-	-	-	-	-	2	-	-	-	3	-	-
CO02	-	-	-	-	-	1	-	2	-	-	-	3	-	-
CO03	-	-	-		-	3	3	3	2	-	-	2	-	-
CO04	-	-	-	-	-	3	-	-	-	-	-	3	-	-
CO05	-	-	-	-	-	2	3	-	-	-	-	2	-	-
CO06	-	-	-	-	-	2	2	2	2	-	-	3	-	-
Total														
Average														

F. SYLLABUS GLIMPSES OF INDIAN CULTURE [P/F]

Course Syllabus

Chapter 1	-	*What is Sanatana Dharma*
Chapter 2	-	*The Heritage ofScriptures*
Chapter 3	-	*The idea of Īśvara*
Chapter 4	-	*Guru Tattva and Avatara Tattva*
Chapter 5	-	*Theory of Karma*
Chapter 6	-	*Purusharthas*
Chapter 7	-	*Sanyasa*
Chapter 8	-	*Yajna*
Chapter 9	-	*Symbolism*
Chapter 10	-	*Understanding Nataraja*
Chapter 11	-	*Temples: The Cradle of Culture*
Chapter 12	-	*Other Heterodox Systems in India*
Chapter 13	-	*Sadhana*

GLIMPSES OF INDIAN CULTURE

Reference Books:

The Eternal Truth by Mata Amritanandamayi Devi
Temples: Centers for Spiritual Practice by Mata Amritanandamayi Devi
All About Hinduism by Swami Sivananda
Art of God Symbolism by Swami Chinmayananda
*Temples in India by Swami Sivanand*a

G. Evaluation Pattern: 60:40

Component	Weightage	Remarks
Internal	60	-
External	40	-
TOTAL	100	